

# High- $Q$ Millimeter Wave RF Filters and Multiplexers

by

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## **AUTHOR'S DECLARATION**

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

# Abstract

For a long period of time, millimeter waves (mm-Wave) were considered unsuitable for wireless data transmission due to high attenuation while propagating in the atmosphere. Over the past few years, due to the vigorous developments of multiple-in-multiple-out (MIMO) antenna technology and semiconductor technology, it is now feasible to have reliable wireless data transmissions using mm-Wave. Traditionally, mobile communication networks operate in the frequency spectrum under 6 GHz. In order to meet the ever-increasing demand for high communication data rate and high-quality multi-media services, the current fifth generation (5G) and the emerging 6G mobile communication systems will start to utilize the mm-Wave spectrum due to its bandwidth advantages, which in turn translates into a high data transmission rate. Millimeter-wave technology is also widely used in radar, imaging, medical therapy, and sensing applications. For those reasons, over the past few years, the interest in mm-Wave spectrum has significantly increased.

RF filters are essential components in any communication systems to provide frequency selectivity. As the operating frequency of communication systems is extending to the mm-Wave spectrum, the conductor loss, the dielectric loss, and the radiation loss increase rapidly, which makes it challenging to develop high- $Q$  mm-Wave filters. Three-dimensional (3D) waveguide filter structures exhibit excellent RF performance at mm-Wave frequencies and have been widely employed in high-performance RF systems. Nevertheless, as the operating frequency increases to mm-Wave frequency, the physical sizes of the waveguide filters become miniature in size impeding the use of post-fabricated tuning elements to compensate for the manufacturing tolerances of the traditional machining technologies. The silicon-micromachining technology has the potential to develop very accurate miniature 3D filters. This thesis focuses on the development of high- $Q$  ultra-wideband mm-Wave planar filters using multilayer superconductor technology and 3D filter structures using silicon micromachining technology, making use of recent advances in deep reactive ions etching (DRIE) techniques.

This thesis first introduces a new technique for filter design and tuning using the phase of the input impedance (PII) as the design parameter. This novel method is applicable to both narrow and wideband filters. Compared with conventional filter design and tuning methods, this approach requires less computation time and provides a clear step-by-step procedure for identifying the proper inter-resonator coupling and the resonant frequencies of the resonators. In practice, the physical realization of the filter always has a non-ideal I/O port, which can introduce an unexpected



unknown transmission line between the physical reference plane and the port of the corresponding inverter in the circuit model. In this thesis, the PII response is used to determine the equivalent electrical length of this unknown transmission line. The validity of the proposed technique is demonstrated through the design of a wideband planar filter with a fractional bandwidth of 72%, the tuning of filters with transmission zeros and the design of a wideband diplexer.

The multilayer superconductor technology allows to realize high- $Q$  planar structures with highly miniature physical dimensions. The superconductor digital receivers can directly digitalize RF signals up to very high frequencies, eliminating the need to use mixers and oscillators to convert the RF signals to lower frequencies. This thesis demonstrates the feasibility of an ultra-wide band superconductor mm-Wave continuous triplexer that can be integrated with superconductor analog to digital converter (ADC) on a single niobium chip. A wideband high- $Q$  mm-Wave highly miniature niobium-based superconductor multiplexer realized on an 8-layer niobium process has been developed, fabricated, and tested covering the frequency range 20 GHz - 80 GHz. In addition to monolithic integration of the superconductor multiplexer with the superconductor ADC, the thesis also demonstrates the feasibility of mounting the triplexer chip on a multi-chip-module (MCM) substrate using flip-chip technology interfaced with 1 mm mm-Wave connectors.

This thesis also demonstrates using a unique behavior of spiral inductors designed intentionally to have a large parasitic capacitance in the realization of a tunable band reject filter. It is shown that, regardless of the operating frequency, the conductivity of the metal strips forming the inductor has a significant impact on how the spiral inductor behaves as an inductor or a capacitor. The concept is used to demonstrate a band reject filter made from a multilayer niobium circuit operating at 4 Kelvin. Such band reject filters are needed in the front-end of superconductor digital receivers to eliminate interference.

Micromachining fabrication processes provide much higher manufacturing accuracy than traditional CNC machining technologies. Moreover, the DRIE silicon micromachining process is more economical for mass production and makes it possible to produce highly accurate 3D waveguide structures. This thesis presents filter designs composing of highly miniature silicon-micromachined ridge waveguide resonators. The proposed filter designs provide highly compact physical size with reasonable high  $Q$  values. An ultra-high- $Q$  mm-Wave cavity filter employing a silicon-micromachined barrel-shape cavities operating in  $TE_{011}$  mode has been developed, fabricated and tested. The barrel-shape is proposed to realize a high- $Q$  cavity, while circumventing the spurious issues of the degenerate TM modes that exist in traditional cylindrical-shape cavities. The filter was realized on silicon using DRIE techniques.

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# Dedication

*“I don’t know anything, but I do know that everything is interesting if you go into it deeply enough.”*

---Richard Feynman

# Table of Contents

Examining Committee Membership.....	ii
AUTHOR'S DECLARATION .....	iii
Abstract .....	iv
Acknowledgements .....	vi
Dedication .....	vii
Table of Contents .....	viii
List of Figures.....	x
Chapter 1 Introduction .....	1
1.1 Motivation.....	1
1.2 Objectives.....	3
1.3 Thesis Outline .....	4
Chapter 2 Literature Review.....	5
2.1 Surface Micromachining and Bulk Micromachining.....	5
2.2 Superconductivity .....	6
2.3 Surface Micromachining Superconductor Filters .....	8
2.4 Bulk Micromachining Filters .....	16
Chapter 3 An Efficient Technique for Design and Tuning of Filters and Diplexers.....	23
3.1 Introduction.....	24
3.2 Design Theory .....	25
3.3 Application of PII Technique to Narrowband Filters .....	28
3.4 Application of PII Technique to Wideband Filters .....	33
3.5 Application of PII Technique to Filters with Transmission Zeros.....	40
3.6 Application of PII Technique to Diplexers .....	47
3.7 Effect of Finite $Q$ .....	53
3.8 Discussion and Conclusion .....	54
Chapter 4 Niobium-Based mm-Wave Ultra-Wideband Filters and Multiplexers.....	58

4.1 Introduction .....	58
4.2 Nb-Based mm-Wave UWB Superconductor Filter.....	60
4.3 Nb-Based mm-Wave Wideband Superconductor Diplexer .....	67
4.4 Nb-Based mm-Wave UWB Superconductor Contiguous Triplexer .....	71
4.5 Integration on Multi-Chip Module (MCM) Substrate with 1 mm Millimeter-wave Connectors.....	79
Chapter 5 Miniature Ultra-Wideband Superconductor Filters with Interference Cancelation ....	86
5.1 Nb-Based Tunable Band Reject Filters.....	86
5.2 Nb-Based UWB Filter with Switchable Notches.....	92
5.3 Nb-based Superconductor Couplers.....	96
Chapter 6 Mm-Wave Silicon-Micromachined Filters .....	101
6.1 Miniature Ridge Waveguide Resonator Filters.....	102
6.2 Ultra-High- $Q$ Cylindrical Cavity Resonator Filter .....	113
6.3 Fabrication of Si-Micromachined Filters .....	123
Chapter 7 Conclusion and Future Work .....	135
7.1 Contributions.....	135
7.2 Future Work .....	136
Reference .....	138
Appendix A Measurement with the Cryogenic RF Probe Station at 4K .....	149
Appendix B Micromachining Fabrication Process .....	154
B.1 RCA Clean .....	154
B.2 Developing a Mask Layer for DRIE .....	155
B.2.1 Using Aluminum as DRIE Hard Mask.....	156
B.2.2 Using SiO <sub>2</sub> as DRIE Hard Mask .....	156
B.2.3 Using Photoresist as DRIE Mask .....	158
B.3 Etching Si Wafers Using DRIE.....	165
B.4 Coating the Metal Layer.....	173

# List of Figures

Fig. 1.1 - 1. The diagram of a RF receiver. ....	2
Fig. 1.1 - 2. The diagram of a superconductor digital receiver. ....	3
Fig. 2.1 - 1. All the surface micromachining processes are performed on the surface of the substrate. ....	5
Fig. 2.1 - 2. Bulk micromachining is used to etch the substrate. ....	5
Fig. 2.2 - 1. The well-known two-fluid model for the superconductor. [7] .....	6
Fig. 2.2 - 2. Variation of surface resistance of copper as a normal conductor and different superconductors vs. frequency [7].....	8
Fig. 2.3 - 1. A cross section of the four-layer surface micromachining fabrication process [10]. .....	9
Fig. 2.3 - 2. (a) The layout of the 3-pole multilayer superconductor filter; (b) the photo of this fabricated filter reported in [10]. ....	9
Fig. 2.3 - 3. The image and schematic of the housing used to test the superconducting chip. [10] .....	9
Fig. 2.3 - 4. The measured results of the 3-pole superconductor filter. [10].....	10
Fig. 2.3 - 5. The 3D layout of the K-band superconductor diplexer and its measured results. [11] .....	10
Fig. 2.3 - 6. The 3-D models of two designs of the 50 $\Omega$ loads and comparison of their input resistance and reactance up to 40 GHz derived from EM simulation results. [11] .....	11
Fig. 2.3 - 7. The layout of the HTS bandstop filter and its equivalent circuit. [12] .....	11
Fig. 2.3 - 8. The measured results of the superconductor switched bandstop filter. [12] .....	12
Fig. 2.3 - 9. Layout of two example resonators composed of double-spiral inductors and interdigital capacitors. The dimensions are in millimeters. [13] .....	13
Fig. 2.3 - 10. Layout of a seven-pole filter using the resonator shown in Fig. 2.3 -9 (Dimensions are in millimeters), and its wide-range simulated and measured results. [13] .....	13
Fig. 2.3 - 11. Photograph of a miniature slot-line resonator filter and its simulated and measured results. [14] .....	14

Fig. 2.3 - 12. The layout of a ultra-narrow band superconductor filer, and its measured result. [15]	15
Fig. 2.4 - 1. The isotropic etching, the anisotropic etching, and the highly anisotropic etching. [17]	17
Fig. 2.4 - 2. The Bosch DRIE process. [20]-[22]	17
Fig. 2.4 - 3. The Octafluorocyclobutane ( $C_4F_8$ ) molecule in plasma has two active ends which allows to form a thin film. [20]-[22]	18
Fig. 2.4 - 4. The layer-by-layer view of a micromachine cavity resonator. [23]	19
Fig. 2.4 - 5. The photograph of a fabricated micromachine cavity resonator filter, and its simulated and measured results. [23]	19
Fig. 2.4 - 6. A micromachining process can be used to fabricate cavity resonator filters. [24].	20
Fig. 2.4 - 7. The X-ray photograph of a fabricated micromachine dual-mode cavity resonator filter and its simulated and measured results. [24]	20
Fig. 2.4 - 8. After including the surface roughness and the non-perfect vertical cavity sidewall profile in the simulation, the simulated results match the measured results well. [24]	20
Fig. 2.4 - 9. The 3D layout of a fourth-order dual-mode cavities filter and the transversal cross-section view of a single cavity. [25]	21
Fig. 2.4 - 10. Longitudinal cross-section view of the proposed 3-layer micromachined filter axially inserted between two waveguide flanges. [25]	22
Fig. 2.4 - 11. The measured and simulated results showing excellent agreement. [25]	22
Fig. 3.1 - 1. Two ideal shunt parallel LC resonators.	24
Fig. 3.2 - 1. Lowpass prototype network and bandpass filter.	26
Fig. 3.3 - 1. Physical layout of three-pole narrowband Chebyshev filter.	28
Fig. 3.3 - 2. The 1 <sup>st</sup> stage physical layout and PII responses.	29
Fig. 3.3 - 3. The 1 <sup>st</sup> PII response after the unknown transition line is removed: $d1 = 0.009$ mm; $L1 = 4.375$ mm; $I0 = 1.5$ mm.	29
Fig. 3.3 - 4. The 2 <sup>nd</sup> stage physical layout.	30
Fig. 3.3 - 5. The 2 <sup>nd</sup> stage RGD responses and PII responses: $d1 = 0.09$ mm; $d2 = 650$ mm; $L1 = 4.375$ mm; $I0 = 1.5$ mm.	30
Fig. 3.3 - 6. The 2 <sup>nd</sup> stage PII responses: $d1 = 0.09$ mm; $d2 = 0.65$ mm; $L1 = 4.375$ mm; <b><math>L2 = 4.415</math> mm</b> ; $I0 = 1.5$ mm.	31

Fig. 3.3 - 7. The 2 <sup>nd</sup> stage PII responses: $d1 = 0.09$ mm; $d2 = \mathbf{0.73}$ mm; $L1 = 4.375$ mm; $L2 = 4.415$ mm; $I0 = 1.5$ mm. ....	31
Fig. 3.3 - 8. Responses of the filter: $d1 = 0.09$ mm; $d2 = 0.73$ mm; $L1 = 4.375$ mm; $L2 = 4.415$ mm; $I0 = 1.5$ mm. ....	32
Fig. 3.4 - 1. Physical layout of CPW ultra-wideband bandpass filter design [40]. ....	33
Fig. 3.4 - 2. The 2 <sup>nd</sup> stage PII responses: $L1 = 1230$ $\mu$ m; $L2 = 1530$ $\mu$ m; $L3 = 1050$ $\mu$ m; $S1=1170$ $\mu$ m; Resonator_1_Length=2430 $\mu$ m; Resonator_2_Length = 2130 $\mu$ m. ....	34
Fig. 3.4 - 3. The 3 <sup>rd</sup> stage PII responses: $L1 = 1350$ $\mu$ m; $L2 = 1650$ $\mu$ m; $L3 = 1290$ $\mu$ m; $L4 = 1230$ $\mu$ m; $L5 = 1080$ $\mu$ m; $S1=1170$ $\mu$ m; $S2 = 930$ $\mu$ m; Resonator_1_Length = 2430 $\mu$ m; Resonator_2_Length = 2250 $\mu$ m; Resonator_3_Length = 2370 $\mu$ m. ....	34
Fig. 3.4 - 4. Responses of the ultra-wideband bandpass filter without final optimization. ....	35
Fig. 3.4 - 5. Responses of the ultra-wideband bandpass filter without final optimization. ....	35
Fig. 3.4 - 6. The lumped circuit model for frequency-dependent inter-resonator coupling. ....	36
Fig. 3.4 - 7. Lumped circuit model for ultra-wideband bandpass filter with frequency-dependent inter-resonator couplings: $C_{S12} = 0.05308$ pF, $L_{S12} = -0.81446$ nH, $C_{S23} = 0.04514$ pF, $L_{S23} = -1.19745$ nH, $C_{S0} = -37.5998$ pF, $L_{S0} = -0.47237$ nH, $C_{P0} = -2C_{S0}$ , $L_{P0} = -0.5L_{S0}$ , $L_1 = 0.32725$ nH, $C_1 = 0.25735$ pF, $L_2 = 0.30367$ nH, $C_2 = 0.28165$ pF, $L_3 = 0.33532$ nH, $C_3 = 0.26492$ pF. ....	36
Fig. 3.4 - 8. Comparison of the lumped LC bandpass filter with conventional coupling matrix. ....	37
Fig. 3.4 - 9. The 1 <sup>st</sup> stage PII responses: $L1 = 2.04$ mm, $W_{Re\_1} = 0.09$ mm, $W_{in} = 0.12$ mm, $Tap\_Open = 0.75$ mm, $Tap\_Short = 0.75$ mm, $Gap = 0.03$ mm. ....	37
Fig. 3.4 - 10. The 2 <sup>nd</sup> stage PII responses: $L1 = 2.19$ mm, $W_{Re\_1} = 0.09$ mm, $W_{in} = 0.12$ mm, $Tap\_Open = 0.45$ mm, $Tap\_Short = 1.2$ mm, $Gap = 0.03$ mm, $L_{12} = 1.32$ mm, $W_{12} = 0.12$ mm, $L2 = 2.01$ mm, $Tap_{12} = 1.2$ mm, $Tap_{21} = 0.96$ mm, $W_{Re\_2} = 0.09$ mm. ....	38
Fig. 3.4 - 11. The 3 <sup>rd</sup> stage PII responses: $L1 = 2.19$ mm, $W_{Re\_1} = 0.09$ mm, $W_{in} = 0.12$ mm, $Tap\_Open = 0.45$ mm, $Tap\_Short = 1.2$ mm, $Gap = 0.03$ mm, $L_{12} = 1.32$ mm, $W_{12} = 0.15$ mm, $L2 = 2.19$ mm, $Tap_{12} = 1.17$ mm, $Tap_{21} = 1.44$ mm, $W_{Re\_2} = 0.09$ mm, $L_{23} = 1.35$ mm, $W_{23} = 0.09$ mm, $L3 = 2.01$ , $Tap_{23} = 1.32$ mm, $Tap_{32} = 0.99$ mm, $W_{Re\_3} = 0.09$ $\mu$ m. ....	39
Fig. 3.4 - 12. Filter responses after the 3 <sup>rd</sup> stage without final fine-tune to compensate for loading effects. ....	39



Fig. 3.5 - 1. Ideal PII responses of the elliptic filter at each design stage. ....	40
Fig. 3.5 - 2. The 2 <sup>nd</sup> stage PII responses of the elliptic filter. ....	41
Fig. 3.5 - 3. The 3 <sup>rd</sup> stage PII responses of the elliptic filter. ....	42
Fig. 3.5 - 4. The last stage PII responses of the elliptic filter. ....	42
Fig. 3.5 - 5. The physical layout of the elliptic filter. ....	43
Fig. 3.5 - 6. Model the non-ideal input port as an ideal transmission line. ....	43
Fig. 3.5 - 7. The 1 <sup>st</sup> stage PII response of the physical filter model after the input coupling is well-tuned. ....	44
Fig. 3.5 - 8. Identifying the equivalent electrical length of the non-ideal input port. ....	45
Fig. 3.5 - 9. PII responses of the new circuit model and the physical model for each design stage of the elliptic filter. ....	45
Fig. 3.5 - 10. The circuit simulation, the measurement results, and the photo of the elliptic filter. ....	46
Fig. 3.6 - 1. Cross-section of two-gold-layer structure. ....	47
Fig. 3.6 - 2. Circuit model of the diplexer. Both coupling matrices have $M_{S1} = M_{4L} = 1.0352$ , $M_{12} = M_{34} = 0.91058$ , $M_{23} = 0.69992$ , and zero the diagonal elements equal to zero. ....	47
Fig. 3.6 - 3. Physical layout of the T-junction and its EM simulation results. ....	48
Fig. 3.6 - 4. Physical layout of the bend and its EM simulation results. ....	48
Fig. 3.6 - 5. Optimized circuit model of the diplexer. Coupling matrix 1: $M_{S1} = 1.0356$ , $M_{12} = 0.94944$ , $M_{23} = 0.71466$ , $M_{34} = 0.91058$ , $M_{4L} = 1.0352$ , $M_{11} = 0.06825$ , $M_{22} = 0.10234$ , $M_{33} = 0.04747$ , $M_{44} = 0$ ; Coupling matrix 2: $M_{S1} = 0.087832$ , $M_{12} = 0.89745$ , $M_{23} = 0.73618$ , $M_{34} = 0.91058$ , $M_{4L} = 1.0352$ , $M_{11} = 0.0297$ , $M_{22} = -0.06897$ , $M_{33} = -0.00389$ , $M_{44} = 0$ ; and zero the diagonal elements equal to zero. ....	49
Fig. 3.6 - 6. Optimized circuit model simulation results. ....	49
Fig. 3.6 - 7. Mapping input couplings of two filters into physical dimensions. ....	50
Fig. 3.6 - 8. The 1 <sup>st</sup> stage PII response of the diplexer. ....	51
Fig. 3.6 - 9. The 2 <sup>nd</sup> stage PII response of the diplexer. ....	51
Fig. 3.6 - 10. The 3 <sup>rd</sup> stage PII response of the diplexer. ....	51
Fig. 3.6 - 11. Mapping the output couplings of the two filters into the physical dimensions. ...	52
Fig. 3.6 - 12. The physical layout of the diplexer after adding the 4 <sup>th</sup> resonators. ....	52
Fig. 3.6 - 13. Circuit model (solid lines) and EM simulation results (dashed lines). ....	53
Fig. 3.7 - 1. The 3 <sup>rd</sup> stage PII response of a 4-pole Chebyshev filter with different $Q$ values. ...	53

Fig. 3.7 - 2. The partial derivatives of the 3 <sup>rd</sup> stage PII for the very low $Q$ filter ( $Q=20$ ).....	54
Fig. 4.1 - 1. The schematic of the SME digital receiver. ....	58
Fig. 4.1 - 2. The cross section of the MIT-LL 8-niobium-layer fabrication process. [50].....	59
Fig. 4.2 - 1. The 3D layout of the multi-layer millimeter-wave UWB bandpass filter. Only the 1 <sup>st</sup> Nb layer is used as the functional signal layer; the subsequent 7 Nb layers are used for additional ground planes and optional crossovers. ....	60
Fig. 4.2 - 2. The CPW resonator with crossovers and its equivalent circuit. ....	61
Fig. 4.2 - 3.(a) EM simulation results for crossovers realized on different Nb layers. (b) EM simulation results for SiO <sub>2</sub> layers with different thickness. ....	62
Fig. 4.2 - 4. EM simulation results for crossovers on the 2nd Nb layer with different widths. .	63
Fig. 4.2 - 5. EM simulation results for the crossovers locate at different places. ....	63
Fig. 4.2 - 6. EM simulation results for the design circuits with two coupled resonators. ....	64
Fig. 4.2 - 7. The 2D layout of the designed mm-Wave superconductor UWB bandpass CPW filter. ....	65
Fig. 4.2 - 8. The fabricated filter was measured with a Lakeshore Cryogenic Probe station.....	66
Fig. 4.2 - 9. The EM simulation and measurement results of the mm-Wave UWB bandpass filter. ....	67
Fig. 4.3 - 1. The 2D layout of the designed mm-Wave wide band superconductor diplexer.....	68
Fig. 4.3 - 2. The EM simulation results of the designed Nb-based mm-Wave wide band superconductor diplexer. ....	68
Fig. 4.3 - 3. (a) The EM simulation results, and (b) the measurement results of the broad band 50 Ohm matched load realized on layer R5. ....	69
Fig. 4.3 - 4. Photo of the fabricated Diplexer.....	70
Fig. 4.3 - 5. Measurement results of the fabricated diplexer.....	70
Fig. 4.4 - 1. The schematic of the mm-Wave UWB triplexer. ....	71
Fig. 4.4 - 2. The 3D layout of the triplexer. Crossovers are built on layer M6. ....	72
Fig. 4.4 - 3. Parasitic parallel-plate modes in between the CPW ground planes. ....	72
Fig. 4.4 - 4. Edge vias are used to suppress the parasitic parallel-plate modes.....	73
Fig. 4.4 - 5. The circuit model of the triplexer includes the filter coupling matrices.....	74

Fig. 4.4 - 6. Dispersion effect and cross talks between channel filters exist in the physical model of the ultra-wide band triplexer. ....	74
Fig. 4.4 - 7. The circuit mode does not take into account the higher propagation modes (harmonics) of the physical filter. ....	75
Fig. 4.4 - 8. Major steps of the design procedure for the proposed UWB triplexer. ....	76
Fig. 4.4 - 9. Flow chart of the hybrid model design procedures. ....	77
Fig. 4.4 - 10. The EM simulation results of the mm-Wave ultra-wide band contiguous triplexer. ....	77
Fig. 4.4 - 11. The fabricated triplexer was measured with a Lakeshore Cryogenic Probe station. ....	78
Fig. 4.4 - 12. Measurement results of the first two channels of the fabricated triplexer. ....	78
Fig. 4.5 - 1. The SME chip can be connected to an antenna outside the cryogenic package via an RF cable. ....	79
Fig. 4.5 - 2. The triplexer is realized on a 4.7 mm x 4.7 mm Nb chip. The Nb chip is assembled on a mother board using the flip-chip technology. Four commercially available RF connectors are assembled with the mother board. ....	79
Fig. 4.5 - 3. The dimensions of the end lunch RF connector operating from DC to 110 GHz. More detailed dimensions of this connector can be found at [52]. ....	80
Fig. 4.5 - 4. Bonding the Nb chip on the mother board by using the wire bonding technology. The diagram is not to scale. ....	80
Fig. 4.5 - 5. Boning the triplexer Nb chip on the mother board by using the flip-chip technology. The diagram is not to scale. ....	81
Fig. 4.5 - 6. The structure of the flip-chip transition. The diagram is not to scale. ....	81
Fig. 4.5 - 7. The EM simulation result of the flip-chip transition structure shown in Fig. 4.5-6. $D_s = H_b = 50 \mu\text{m}$ . $G_b = 350 \mu\text{m}$ . The length of the 50 Ohm CPW line on the Nb chip is 494 $\mu\text{m}$ . The length of the 50 Ohm GCPW line on the mother board is 7.9 mm. ....	82
Fig. 4.5 - 8. The basic equivalent circuit model for the flip-chip interconnection with the loss ignored. [58] ....	82
Fig. 4.5 - 9. The EM simulation results of the flip-chip transition structure shown in Fig. 4.5-6 with the height of the bumps swept. All the three bumps have the identical diameter of 50 $\mu\text{m}$ . The length of the 50 Ohm CPW line on the Nb chip is 494 $\mu\text{m}$ . The length of the 50 Ohm GCPW line on the mother board is 7.9 mm. ....	83

Fig. 4.5 - 10. The EM simulation results of the flip-chip transition structure shown in Fig. 4.5-6 with the diameters of the bumps swept. The height of the bumps is 50 $\mu\text{m}$ . The length of the 50 Ohm CPW line on the Nb chip is 494 $\mu\text{m}$ . The length of the 50 Ohm GCPW line on the mother board is 7.9 mm. ....	83
Fig. 4.5 - 11. The EM simulation results of the flip-chip transition structure shown in Fig. 4.5-6 connected with the connector. The height of the bumps is 80 $\mu\text{m}$ and the diameter of the bumps is 50 $\mu\text{m}$ . The length of the 50 Ohm CPW line on the Nb chip is 494 $\mu\text{m}$ . The length of the 50 Ohm GCPW line on the mother board is 7.9 mm. The encrypted HFSS model of the connector is provided by Southwest Microwave Inc. ....	84
Fig. 4.5 - 12. The EM simulation results of the Nb-based triplexer. The Nb chip is mounted on the motherboard by using the flip-chip technology and RF connectors are assembled with the mother board.....	84
Fig. 4.5 - 13. The photo of the triplexer chip mounted on an MCM substrate using flip-chip technology interfaced with 1 mm mm-Wave connectors. ....	85
Fig. 5.1 - 1. The schematic of the tunable band reject filter circuit. ....	87
Fig. 5.1 - 2. Equivalent circuit model of a lumped spiral inductor. ....	87
Fig. 5.1 - 3. Two Nb spiral with different physical dimensions.....	89
Fig. 5.1 - 4. EM simulation results of the two spiral structures in Fig. 5.1-3.....	89
Fig. 5.1 - 5. The 3D layout of the proposed lumped-element Nb-based superconducting tunable band stop filter.....	90
Fig. 5.1 - 6. The measurement results of a single band stop filter operates at the superconducting state.....	90
Fig. 5.1 - 7. The measurement results of a single band stop filter when DC current is applied to the Nb spiral inductor. ....	90
Fig. 5.1 - 8. Photo of the fabricated tunable band reject filter circuit. ....	91
Fig. 5.1 - 9. (a) The measurement results when one rejection band is turned off. (b) The measurement results when two rejection bands are turned off simultaneously.....	91
Fig. 5.2 - 1. The schematic block diagram of a superconductor RF front-end.....	92
Fig. 5.2 - 2. The schematic of the stepped-impedance multimode resonator.....	93
Fig. 5.2 - 3. The schematic of a mm-Wave UWB filter with one SIR MMR. ....	93
Fig. 5.2 - 4. The cross section of the MIT-LL 4-Nb-layer fabrication process. [49] .....	93

Fig. 5.2 - 5. (a) The EM-simulation result of the mm-Wave UWB triple-mode-resonator filter shown in Fig. 5.2-3. (b) The EM-simulation result of the mm-Wave UWB triple-mode-resonator filter shown in Fig. 5.2-3. ....	94
Fig. 5.2 - 6. The EM simulations results for the Nb in the spiral inductor operating in the superconducting state and the normal conductor state. ....	94
Fig. 5.2 - 7. The measurement results of the band reject filter with/without DC current applied to the spiral inductor. ....	94
Fig. 5.2 - 8. The cascaded EM simulation results of the Nb-based mm-Wave MMR UWB bandpass filter with a switchable notch. (a). The spiral inductor in the band reject filter operates in the superconducting state. (b). The spiral inductor in the band reject filter operates in the normal conductor state. ....	95
Fig. 5.2 - 9. The cascaded measurement simulation results of the Nb-based mm-Wave MMR UWB bandpass filter with a switchable notch. (a). The spiral inductor in the band reject filter operates in the superconducting state. (b). The spiral inductor in the band reject filter operates in the normal conductor state. ....	96
Fig. 5.3 - 1. The schematic of a designed Nb-based mm-Wave UWB 3 dB Lange coupler. ....	97
Fig. 5.3 - 2. The simulation results of the Nb-based mm-Wave UWB 3 dB Lange coupler. ....	97
Fig. 5.3 - 3. The the 3D layout of the designed Nb-based mm-Wave UWB 3 dB Lange coupler. ....	98
Fig. 5.3 - 4. The photos of the fabricated Lange couplers with 50 Ohm loads at different ports. ....	98
Fig. 5.3 - 5. The the measurement results of the designed Nb-based mm-Wave UWB 3 dB Lange coupler. ....	98
Fig. 5.3 - 6. The 2D layout of a Nb-based 30 dB coupler which is realized by cascading two 15 dB coupled line couplers. ....	99
Fig. 5.3 - 7. The EM simulation results of the Nb-based 30 dB coupler. ....	99
Fig. 5.3 - 8. The photo of the fabricated Nb-based 30 dB couplers with 50 Ohm loads at different ports. ....	100
Fig. 5.3 - 9. The measurement results of the Nb-based 30 dB coupler. ....	100
Fig. 6.0 - 1. The photo of a designed structure was fabricated by cutting the stainless steel with the CNC laser machine and by etching the Si wafer with the DRIE micromachining process. ....	101

Fig. 6.1- 1. The dimensions of an air-filled gold cavity resonator and an alumina-filled gold cavity resonator with the 1 <sup>st</sup> resonant mode at 25.5 GHz. ....	103
Fig. 6.1- 2. The dimensions of a single ridge waveguide resonator with the 1 <sup>st</sup> resonant mode at 25.5 GHz.....	104
Fig. 6.1- 3. The dimensions of a dielectric loaded double-ridge waveguide resonator with the 1 <sup>st</sup> resonant mode at 25.5 GHz.....	104
Fig. 6.1- 4. Comparing the dimensions of an air-filled gold cavity resonator with a dielectric loaded double-ridge waveguide resonator. The 1 <sup>st</sup> modes of both resonators are at 25.5 GHz...	104
Fig. 6.1- 5. The dimensions of a dielectric loaded double-T-Septum waveguide resonator with the 1 <sup>st</sup> resonant mode at 20 GHz. ....	105
Fig. 6.1- 6. The 3D view and the layer-by-layer view of an mm-Wave dielectric loaded double-T-Septum waveguide resonator filter. ....	106
Fig. 6.1- 7. The simulation results of the mm-Wave dielectric loaded double-T-Septum waveguide resonator filter. ....	106
Fig. 6.1- 8. The dimensions of the top part of the mm-Wave dielectric loaded double-T-Septum waveguide resonator filter. ....	107
Fig. 6.1- 9. The dimensions of the bottom part of the mm-Wave dielectric loaded double-T-Septum waveguide resonator filter. ....	107
Fig. 6.1- 10. The dimensions of the middle part of the mm-Wave dielectric loaded double-T-Septum waveguide resonator filter. ....	108
Fig. 6.1- 11. The 3D view and the layer-by-layer view of a wideband dielectric loaded double-T-Septum waveguide resonator filter. ....	109
Fig. 6.1- 12. The simulation results of the wideband dielectric loaded double-T-Septum waveguide resonator filter. ....	109
Fig. 6.1- 13. The dimensions of the top part of the wideband dielectric loaded double-T-Septum waveguide resonator filter. ....	110
Fig. 6.1- 14. The dimensions of the bottom part of the wideband dielectric loaded double-T-Septum waveguide resonator filter. ....	110
Fig. 6.1- 15. The dimensions of the bottom part of the wideband dielectric loaded double-T-Septum waveguide resonator filter. ....	111
Fig. 6.1- 16. The 3D view, the layer-by-layer view and the simulation results of a Sub-6GHz dielectric loaded double-T-Septum waveguide resonator filter.....	112

Fig. 6.1- 17. The electric field distributions of the low and high modes for the positive coupling structure used in the Sub-6GHz dielectric loaded double-T-Septum waveguide resonator filter. ....	113
Fig. 6.1- 18. The electric field distributions of the low and high modes for the negative coupling structure used in the Sub-6GHz dielectric loaded double-T-Septum waveguide resonator filter. ....	113
Fig. 6.2 - 1. Atmospheric losses as a function of frequency. [78] .....	114
Fig. 6.2 - 2. $Q$ factor for different modes and the mode chart for a circular cylindrical cavity. [83] .....	115
Fig. 6.2 - 3. Current distribution for the TE <sub>011</sub> mode and TM <sub>111</sub> mode of a circular cylindrical cavity. ....	116
Fig. 6.2 - 4. The schematics of the published barrel-shape cavity resonator in [65] and the proposed cavity resonator with stepped inclined sidewalls.....	116
Fig. 6.2 - 5. Simulations of a cylindrical cavity resonator and a proposed stepped inclined sidewall cylindrical cavity resonator. ....	117
Fig. 6.2 - 6. Simulation of a cylindrical cavity resonator with four silver posts. ....	117
Fig. 6.2 - 7. The 3D view and the layer-by-layer view of a stepped inclined sidewall cylindrical cavity resonator filter.....	118
Fig. 6.2 - 8. The simulation results of a stepped inclined sidewall cylindrical cavity resonator filter. ....	118
Fig. 6.2 - 9. The dimensions of the cavity structures for the stepped inclined sidewall cylindrical cavity resonator filter built on Si wafers. ....	119
Fig. 6.2 - 10. The dimensions of the input/output of the stepped inclined sidewall cylindrical cavity resonator filter.....	120
Fig. 6.2 - 11. A defected ground microstrip line is used to excite the TE <sub>01</sub> mode of a cylindrical cavity resonator. ....	121
Fig. 6.2 - 12. The inter-resonator coupling between two cylindrical cavity resonators can be realized by using a rectangular waveguide.....	122
Fig. 6.2 - 13. A very-high- $Q$ TE <sub>011</sub> mode cylindrical cavity filter is designed at the center frequency of 229.4 GHz with a fractional bandwidth of 0.1%.....	122
Fig. 6.3 - 1. The micromachining process was used to make cavities on Si wafers for the T-septum filters designed in Section 6.1. ....	123

Fig. 6.3 - 2. The photo of a 4-inch Si wafer coated with 15 $\mu\text{m}$ thick positive photoresist and the edge bead is removed. ....	124
Fig. 6.3 - 3. The Si wafers with patterned photoresist layers used for developing the filter shown in Fig. 6.1-6 and Fig. 6.1-12. ....	124
Fig. 6.3 - 4. The Si wafer shown in Fig. 6.3-3 were etched by using DRIE. ....	125
Fig. 6.3 - 5. (a) The metallized Si pieces for developing the filter shown in Fig. 6.1-6. (b) The metallized Si pieces for developing the filter shown in Fig. 6.1-12. ....	125
Fig. 6.3 - 6. The micromachining process was used to make cavities on Si wafers for the barrel-shape cavity resonator filter filter designed in Section 6.2. ....	126
Fig. 6.3 - 7. The Si wafer was first etched by using DRIE to make the designed patterns have a depth of 400 $\mu\text{m}$ . ....	126
Fig. 6.3 - 8. The smaller Si piece was mounted on a carrier wafer for the final etching through process. ....	127
Fig. 6.3 - 9. The photo of the etched through Si pieces used for developing the barrel shape cavity resonator filter. ....	127
Fig. 6.3 - 10. The photo of the metallized etched through Si pieces. ....	128
Fig. 6.3 - 11. The photo of the fabricated alumina substrate (top). ....	128
Fig. 6.3 - 12. The photo of the fabricated alumina substrate (bottom). ....	129
Fig. 6.3 - 13. The EM simulation and the measurement results of the micromachined dielectric-loaded wideband filter shown in Fig. 6.1-11. ....	129
Fig. 6.3 - 14. The EM simulation and the measurement results of the micromachined dielectric-loaded wideband filter shown in Fig. 6.1-6. ....	130
Fig. 6.3 - 15. The micromachined dielectric-loaded filters were assembled by using a Tresky T-3000-FC3 Die Bonder [86] with epoxy (EPO-TEK® H20E) as the adhesive ....	131
Fig. 6.3 - 16. The EM simulations results demonstrate the effect of the thickness of epoxy thickness affects the filter performance significantly. ....	132
Fig. 6.3 - 17. The EM simulation and the measurement results of the micromachined barrel-shape cavity resonator filters shown in Fig. 6.2-7. ....	132
Fig. 6.3 - 18. The photo and the schematic of the cross-section of the DRIE micromachined silicon trench. ....	133
Fig. 6.3 - 19. The EM simulation results of the micromachined barrel-shape cavity resonator filters shown in Fig. 6.2-7 with the radiuses shown in Fig. 6.2-9 increased by 200 $\mu\text{m}$ . ....	134



# Chapter 1

## Introduction

### 1.1 Motivation

The millimeter wave (mm-Wave) spectrum covers the radio frequency (RF) band from 30 GHz to 300 GHz. Because radio waves within this band have wavelengths from one to ten millimeters, they are referred to as millimeter waves. Mm-Wave technology can be applied to many different fields. Conventionally, mobile communication systems have used the frequency spectrum under 6 GHz, but this is now almost fully occupied. Consequently, the current fifth generation (5G) and emerging sixth generation (6G) mobile communication systems will begin to utilize the mm-Wave spectrum to meet the ever-growing demands for high communication data rate and high-quality multimedia services. When used for terrestrial communication applications, mm-Wave suffers severe attenuation when propagating in the atmosphere. Thus, mm-Wave can only be used for short-distance wireless communications. On the other hand, short-range communications can improve spectrum utilization through frequency reuse over a small coverage area. In addition, a small coverage area is conducive to building a secure local wireless communication network, since the hackers cannot tap into the data stream. Another useful application of mm-Wave technology is communication between satellites. For example, although the energy of a 60 GHz mm-Wave can be absorbed by oxygen in the atmosphere, there is almost no oxygen in high Earth orbit, so the 60 GHz mm-Wave is a perfect candidate for communication in this region, with the added benefit of massive data rate and low latency between satellites. In addition to communications, millimeter wave technology is also widely used in other fields, such as radar, imaging, medical therapy, and sensing. For all of these reasons, interest in mm-Wave spectrum has significantly increased over the past few years [1]-[6].

Radio frequency filters are used to provide frequency selectivity in RF systems by passing through the desired signals and rejecting the unexpected signals. Figure 1.1-1 depicts an RF receiver used in a typical RF communication system. As can be seen, the insertion loss of the RF filters significantly affects the overall performance of the entire RF system, particularly its over-noise performance, since the insertion loss of the front-end filter contributes directly to the overall system noise figure. Therefore, high- $Q$  filters, which have low-insertion loss levels, are always

needed for RF communication systems. As the operating frequency increases to the mm-Wave spectrum, the conductor loss, dielectric loss, and radiation loss increase rapidly, which makes it challenging to develop high- $Q$  RF filters.

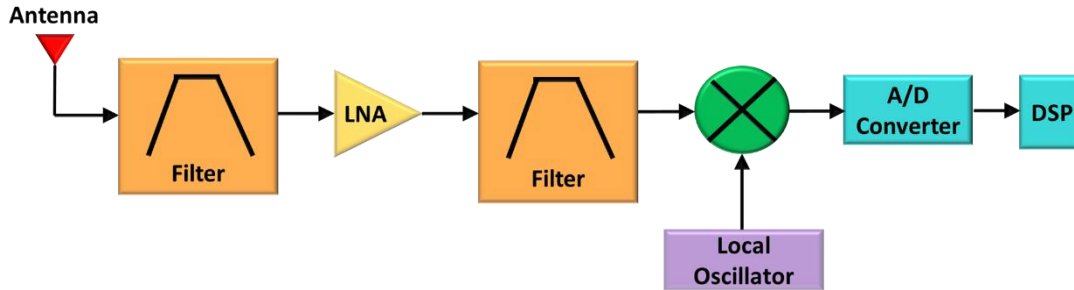


Fig. 1.1 - 1. The diagram of a RF receiver.

Conventionally, coaxial combline filters have been widely used in base stations in previous generations' communication systems (i.e., 1G – 4G) to achieve compact physical size. However, as the operating frequencies of the current 5G and emerging 6G systems expand to the mm-Wave spectrum, the  $Q$ -values of combline filters deteriorate severely, resulting in a drastically attenuated signal. Waveguide filters exhibit excellent RF performance at mm-Wave frequencies and are widely employed in high-performance RF systems. These filters are fabricated on metal blocks by using computer numerical controlled (CNC) machining technologies. Unfortunately, due to their low manufacturing accuracy, waveguides filters are always equipped with tuning screws for post-fabrication tuning. As the operating frequency increases to mm-Wave frequency, the physical sizes of the waveguide filters become compact and do not allow for the installation of tuning elements to compensate for the manufacturing inaccuracy of CNC machining technologies.

With the recent development of the silicon deep reactive ions etching (DRIE) technology, waveguide filters can be implemented on silicon wafers. DRIE is a bulk micromachining technology that uses chemical and molecule level physical treatments to construct waveguides on a silicon wafer. This gives it much higher manufacturing accuracy than the CNC machining technologies. Moreover, the DRIE process is relatively uncomplicated and cost-effective, making it highly desirable for developing high- $Q$  mm-Wave waveguide filters.

Nowadays, with the development of Superconductor Micro-Electronic (SME) technology, superconductor digital receivers can directly digitalize RF signals up to very high frequencies. They even have the potential to directly digitalize RF signals up to several hundred gigahertz without the need to use mixers and oscillators to convert the RF signals to lower frequencies. By using SME technology, the RF receiver systems shown in Fig.1.1-1 can be greatly simplified, as presented in

Fig. 1.1-2. In addition, superconductors have much lower surface resistance than ordinary conductors, allowing the technology to realize high-performance mm-Wave filters with compact physical size. The highly miniature superconductor filter can be monolithically integrated with the superconductor analog-to-digital converter (ADC), enabling a highly miniaturized superconductor digital receiver (shown in Fig. 1.1-2) to be realized on a single chip.

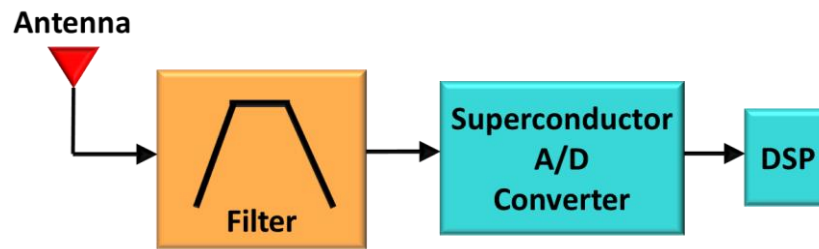


Fig. 1.1 - 2. The diagram of a superconductor digital receiver.

## 1.2 Objectives

This thesis focuses on the development of highly miniaturized high- $Q$  planar structure filters and multiplexers by using niobium-based superconducting technology, and the development of silicon-micromachined high- $Q$  millimeter-wave filters by using DRIE technology. In this thesis, both DRIE technology and superconducting technology are used to develop highly miniature high- $Q$  filters for Sub-7GHz and mm-Wave applications. The main objectives of the thesis are:

- Development of an efficient technique for the design and tuning of filters and multiplexers that circumvents the shortcomings of the conventional filter design methods.
- Development of highly miniature high- $Q$  superconductor niobium-based mm-Wave ultra-wideband filters and multiplexers covering the frequency range from 20 GHz to 80 GHz.
- Development of novel switchable band reject filters for integration with wideband superconductor filters for interference cancelation.
- Development of silicon micromachined millimeter-wave filters by using the DRIE technology.

## 1.3 Thesis Outline

The motivation and objectives of this thesis are described in Chapter 1. Chapter 2 discusses background information on superconductors and the micromachining process. It also highlights the superconductor filters and micromachining filters reported in the literature. Chapter 3 presents a new filter design methodology developed during the research that can be used to design and tune filters and diplexers very efficiently. Chapter 4 describes the research activities of the proposed highly miniature niobium-based mm-Wave ultra-wideband contiguous triplexer with a frequency coverage from 20 GHz to 80 GHz. Chapter 5 provides details on the research activities of the proposed novel switchable band reject filter. Chapter 6 delves into the research activities of the proposed Si-based micromachining filters. Finally, Chapter 7 concludes the thesis by summarizing the results achieved, followed by proposals for future research.

# Chapter 2

## Literature Review

In this chapter, A literature review of background information and relevant material will be presented. First, section 2.1 will briefly discuss the difference between surface micromachining and bulk micromachining. Section 2.2 will review superconductivity, while highlighted published superconductor filters will be reviewed in section 2.3. Finally, section 2.4 will review RF filters that are realized using micromachining technologies.

### 2.1 Surface Micromachining and Bulk Micromachining

Generally, micromachining techniques can be compartmentalized into two main categories: surface micromachining and bulk micromachining. In surface micromachining (as shown Fig 2.1-1), all fabrication processing is performed on top of the substrate by alternatively depositing and patterning the dielectric and conductor layers on the surface of the substrate. The additive layers on top of the substrate can have a total thickness from several nanometers to several micrometres. Normally, surface micromachining techniques are used to develop planar transmission line

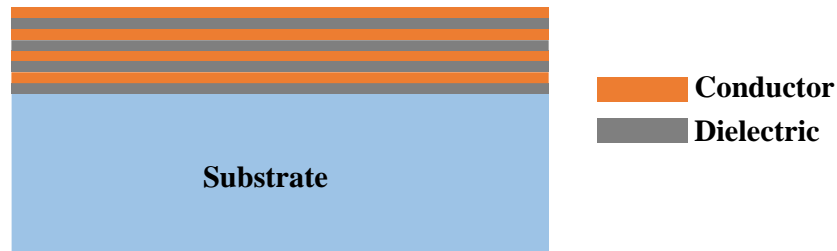


Fig. 2.1 - 1. All the surface micromachining processes are performed on the surface of the substrate.

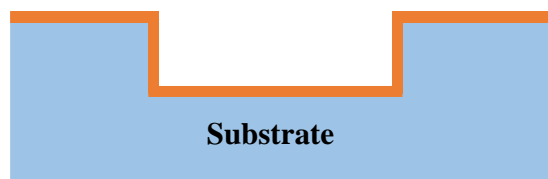


Fig. 2.1 - 2. Bulk micromachining is used to etch the substrate.

structures. If using superconductors in surface micromachining, compact high- $Q$  planar transmission line resonators can be realized.

In bulk micromachining (as shown in Fig. 2.1-2), the substrate is etched by using wet chemical etching or plasma etching techniques. Several etched substrates can be stacked together to form a waveguide that can have a height from several micrometers to several millimeters. Nowadays, bulk micromachining is widely used to build wafer-level cavity resonators for high frequency applications.

## 2.2 Superconductivity

Superconductors have several attractive features. For RF filter engineers, the most attractive of these for superconductors is their extremely low resistance, which allows for the realizing of miniature RF resonators with high- $Q$  values.

Ordinary conductors only contain electrons, which means that the current is carried by electrons. Superconductors contain electrons and electron pairs (known as Cooper pairs), both of which can carry a current. When travelling in conductors, electrons experience resistive losses, whereas Cooper pairs do not. In superconductors, the ratio between the number of electrons and Cooper pairs varies by temperature. When the temperature falls below the superconductor's critical temperature, Cooper pairs begin to form; as the temperature goes down further, the number of Cooper pairs in the superconductor increases. Equation 2.1 expresses the relationship between the number of electrons ( $n_n$ ) and the number of Cooper pairs ( $n_s$ ) in a superconductor.

$$\begin{aligned} n_s &= n_0 \left(1 - \left(\frac{T}{T_c}\right)^4\right), \\ n_n &= n_0 \left(\frac{T}{T_c}\right)^4 \end{aligned} \quad (2.1)$$

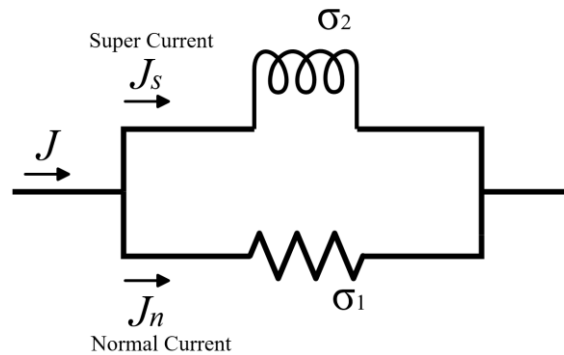


Fig. 2.2 - 1. The well-known two-fluid model for the superconductor. [7]

As shown in the above equation,  $n_0$  denotes the total number of carriers in the superconductor,  $T_C$  is the critical temperature of the superconductor, and  $T$  is the actual temperature.

Figure 2.2-1 depicts the well-known equivalent circuit model (known as the two-fluid model) for the superconductor. The total current density is denoted as  $J$ . In the two-fluid model, the total current is split into the super current and the normal current.  $J_n$  denotes the normal current density carried by the electrons, and  $J_s$  denotes the super current density carried by Cooper pairs. The complex conductivity of the superconductors can be expressed as  $\sigma_1 - j\sigma_2$ . At the direct current (DC), the inductor becomes a short circuit. As the frequency increases, the reactance grows. The impedance of the superconductor can be expressed as:

$$Z_S = \frac{\omega^2 \mu^2 \sigma_1 \lambda_{PD}^3}{2} + j\omega \mu \lambda_{PD}. \quad (2.2)$$

Here,  $\lambda_{PD}$  denotes the penetration depth of the superconductor, which is inversely proportional to the operating frequency and  $\sigma_2$ . Thus, the penetration depth of the superconductors is much smaller than the skin depth of the normal conductors at typical RF and mm-Wave frequencies. The detailed derivation process of Equation (2.2) can be found in [7] and [8]. As shown in Equation (2.2), the surface resistance (the real part of  $Z_S$ ) of the superconductor increases as the square of the frequency. For ordinary conductors, surface resistance can be expressed as:

$$R_{S\_ordinary} = \sqrt{\frac{\omega \mu}{2\sigma_n}}, \quad (2.3)$$

with surface resistance increasing the square root of the frequency.

Equations (2.2) and (2.3) reveal that, as the frequency increases, the surface resistance of the superconductor increases more rapidly than that of the ordinary conductor. At low frequencies, a superconductor has much less surface resistance than an ordinary conductor. However, as the frequency increases, superconductor surface resistance will eventually become larger than ordinary conductor surface resistance.

Figure 2.2-2 shows a comparison of variations in surface resistance versus frequency for superconductors (YBCO at 77K and Nb at 7.7K) and an ordinary conductor (copper at 77K). As seen in the figure, the high-temperature superconductor (HTS) yttrium barium copper oxide (YBCO) at 77K has the same surface resistance of around 200 GHz as the ordinary conductor copper at 77K. The low-temperature superconductor, niobium (Nb) at 7.7K, has the same surface resistance as the copper at 77K when the frequency is around 1 THz. At typical RF and mm-Wave frequencies under 100 GHz, Nb at 7.7K has much less surface resistance than ordinary conductors.

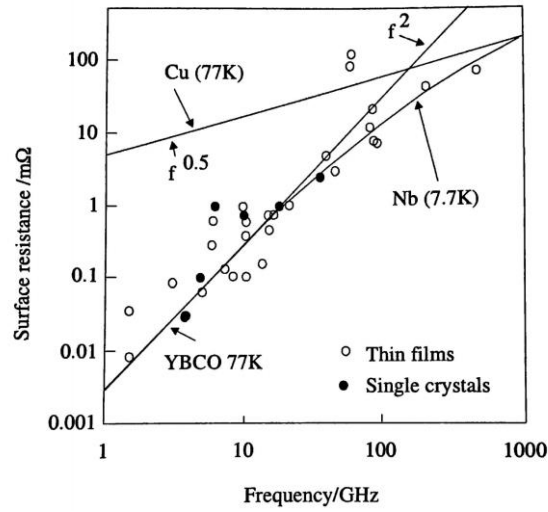


Fig. 2.2 - 2. Variation of surface resistance of copper as a normal conductor and different superconductors vs. frequency [7].

## 2.3 Surface Micromachining Superconductor Filters

Surface micromachining techniques are normally employed to develop lumped-element and planar transmission-line resonators. These two resonator types have compact physical size in comparison to 3D cavity and dielectric resonators. However, lumped-element and planar transmission-line resonators have low- $Q$  values due to high ohmic losses. By using ordinary conductors, the typical  $Q$  value for a lumped-element resonator is below 50 at 1 GHz, while the typical  $Q$  value for planar transmission-line resonators is in the range of 50 - 300 at 1 GHz [9]. The low- $Q$  characteristics limit the use of the lumped-element and planar transmission-line resonators in high- $Q$  applications. By combining surface micromachining and superconducting techniques, highly miniature high- $Q$  filters can be realized. In this section, highlighted publications about surface micromachining superconductor filters will be reviewed.

In [10], a highly miniaturized high- $Q$  multilayer niobium-based (Nb-based) superconductor lumped-element resonator filter is reported. The filter was realized by using a four-layer surface micromachining process, as shown in Fig. 2.3-1. In this process, layers M0 – M3 are the superconductor layers. As depicted in Fig. 2.3-2, the lumped capacitors were developed on different superconductor layers to achieve a super-compact physical size. The size of each resonator is 0.5 mm x 0.55 mm which is only 1/500 of the wavelength at the filter's center frequency. This resonator is probably the smallest RF resonator in existence thus far.



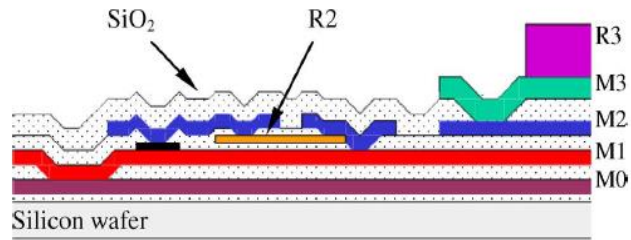


Fig. 2.3 - 1. A cross section of the four-layer surface micromachining fabrication process [10].

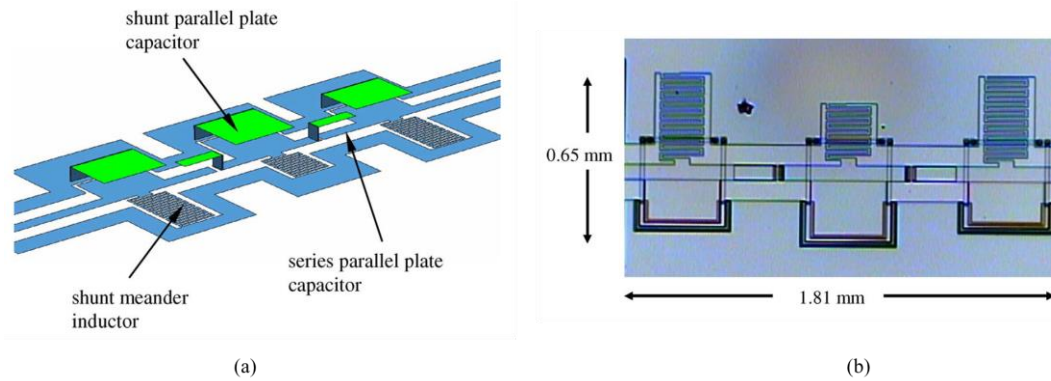


Fig. 2.3 - 2. (a) The layout of the 3-pole multilayer superconductor filter; (b) the photo of this fabricated filter reported in [10].

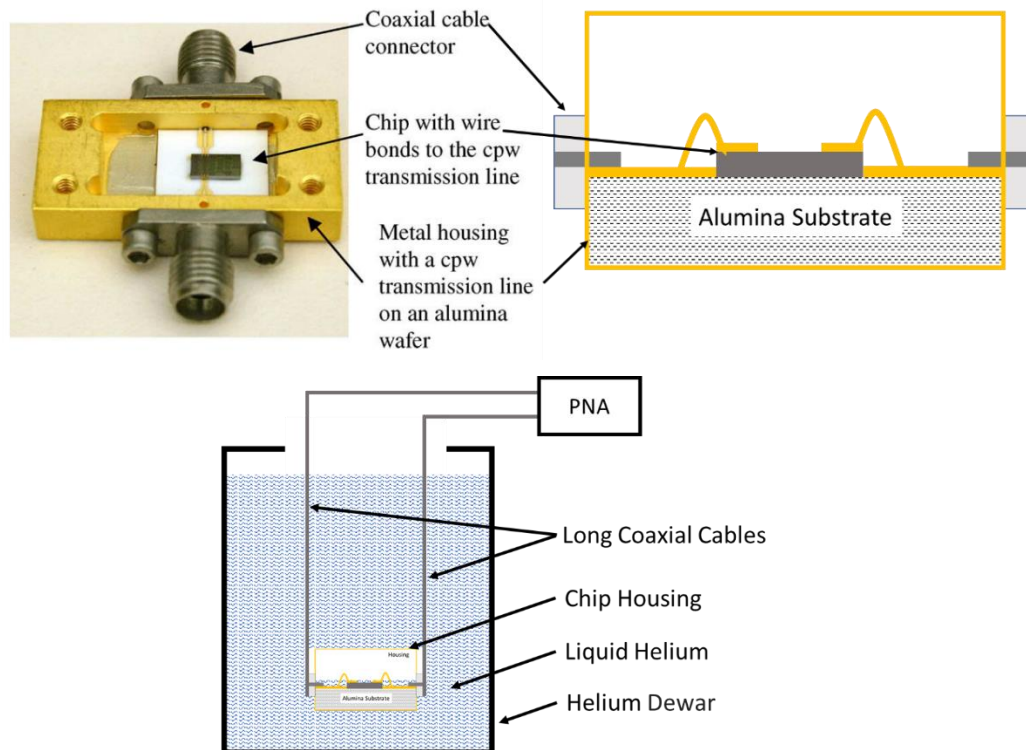


Fig. 2.3 - 3. The image and schematic of the housing used to test the superconducting chip. [10]

To measure the filter, the Nb chip is wire-bound on an alumina substrate placed in a metal housing, as shown in Fig. 2.3-3. Then, the coaxial cables and the metal housing is immersed in liquid helium to make the Nb operate at the superconducting state. The measurement results of this filter are given in Fig. 2.3-4. As can be seen, the insertion loss within the passband is around 0.26 dB, which includes the losses caused by the coaxial cables, CPW line on the alumina substrate and wire bounds. This Nb filter shows that micromachining superconducting techniques allows super-compact RF filters to be realized with superior performance.

The micromachining process illustrated in Fig. 2.3-1 was also used to develop a multilayer K-band diplexer [11]. The 3D model and the measurement results of this K-band diplexer are shown in Fig. 2.3-5. To measure the three-port diplexer with an RF probe station using only two RF probes, one port of the diplexer should be terminated to 50 Ohm when the other two ports are being measured. In [11], a broadband match load is developed by using the lossy conductor layer (R2) in

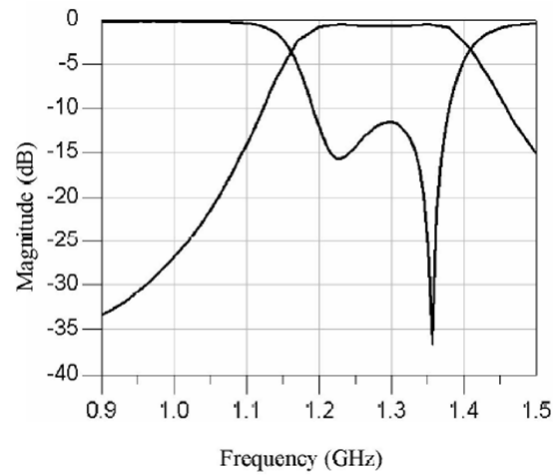


Fig. 2.3 - 4. The measured results of the 3-pole superconductor filter. [10]

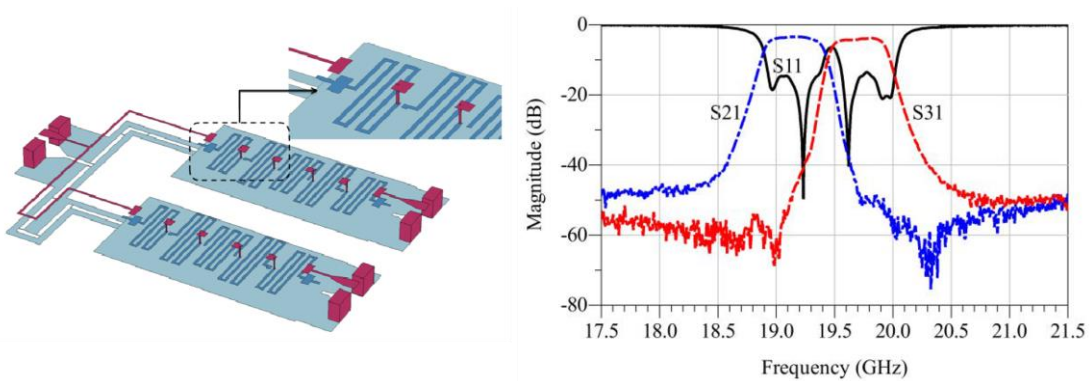


Fig. 2.3 - 5. The 3D layout of the K-band superconductor diplexer and its measured results. [11]

the micromachining process presented in Fig. 2.3-1. As shown in Fig. 2.3-6, this broadband match load consists of a meander lossy conductor line and a floating metal plate underneath, which are used to eliminate the parasitic reactance of the straight resistive line. The proposed broadband match load structure has a constant resistance and zero reactance from DC to 40 GHz. By using this ideal, a 50 Ohm match load from DC to 90 GHz was developed and will be presented in Chapter 4. As will be seen in Chapters 4 and 5, the broadband match loads are very useful for measuring broadband multiplexers and developing broadband RF couplers.

Another feature of the superconductor is its switching capabilities, which allows the superconductor filter to operate as a switch. The literature [12] demonstrated this feature of the superconductor

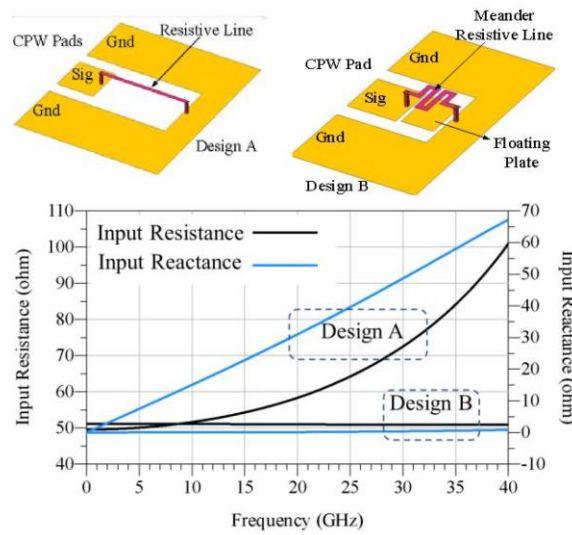


Fig. 2.3 - 6. The 3-D models of two designs of the 50  $\Omega$  loads and comparison of their input resistance and reactance up to 40 GHz derived from EM simulation results. [11]

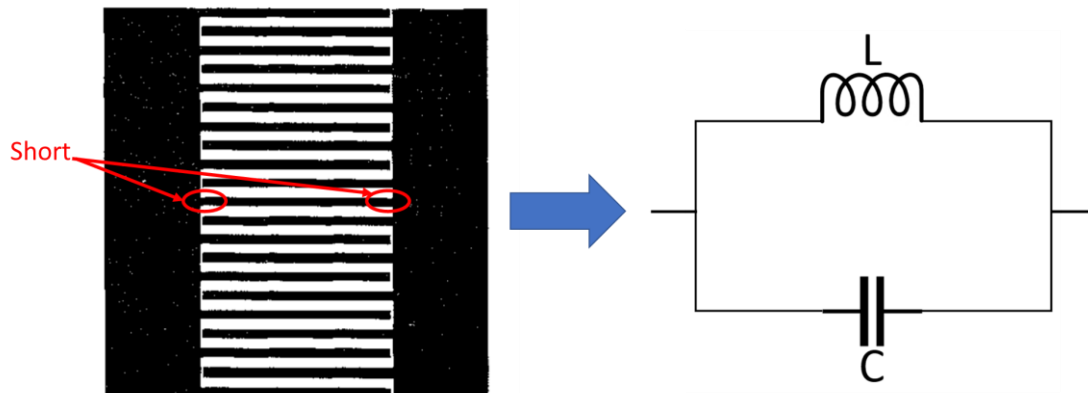


Fig. 2.3 - 7. The layout of the HTS bandstop filter and its equivalent circuit. [12]

filter already in 1996. Figure 2.3-7 depicts an HTS bandstop filter. When the conductor operates in the superconducting state, this structure is the equivalent of a parallel LC circuit and thus functions as a bandstop filter. When a bias DC is applied to the superconductor filter, the current density is over the critical current density of the superconductor and thus turns it into a normal conductor with high resistance. As shown in Fig. 2.3-8, the structure operates as a bandstop filter when no bias DC is applied. However, when a bias DC is applied, the resonance that provides the bandstop function no longer exists and this structure operates as a lossy all-pass filter. As will be explained in Chapter 5, a tunable band reject filter is developed by using a bias DC to control the operating state of the superconductor.

In [13], the authors propose microstrip resonators that have symmetrical double-spiral (spiral-in/spiral-out) inductors and interdigital capacitors, as shown in Fig. 2.3-9. Within these resonators, most of the electric energy is stored in the interdigital lines, while most of the magnetic energy is stored in the double-spiral lines. By using HTS as a conductor, the resonators have a very high- $Q$  value of 200,000 at 0.61 GHz, while also having a compact physical size of only 1/100 of the wavelength at the resonant frequency. A 7-pole bandpass filter with a fractional bandwidth of 0.8% at the center frequency of 0.61GHz was realized by using the proposed resonators. As provided in Fig. 2.3-10, this proposed bandpass filter has a wide spurious free window between the fundamental passband and the 2<sup>nd</sup> harmonic passband.

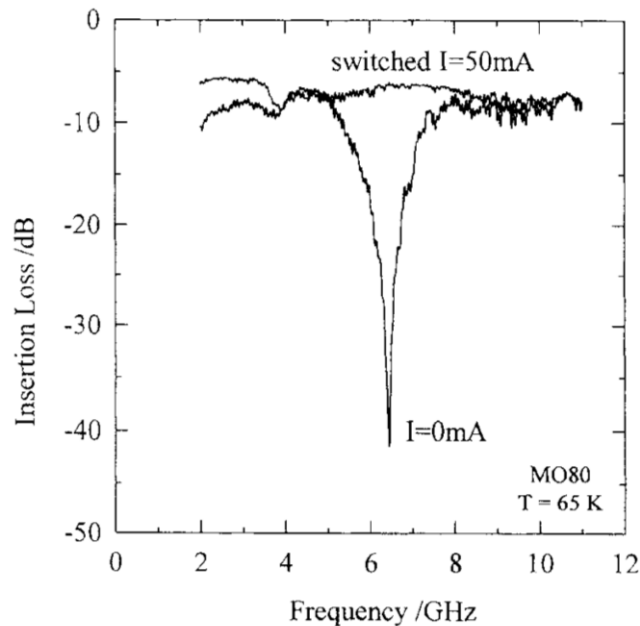


Fig. 2.3 - 8. The measured results of the superconductor switched bandstop filter. [12]

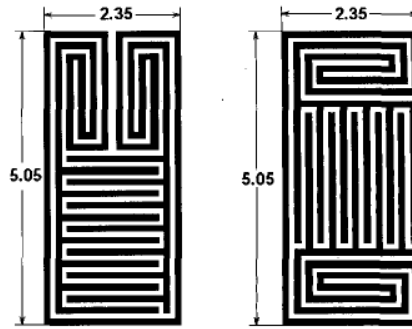


Fig. 2.3 - 9. Layout of two example resonators composed of double-spiral inductors and interdigital capacitors. The dimensions are in millimeters. [13]

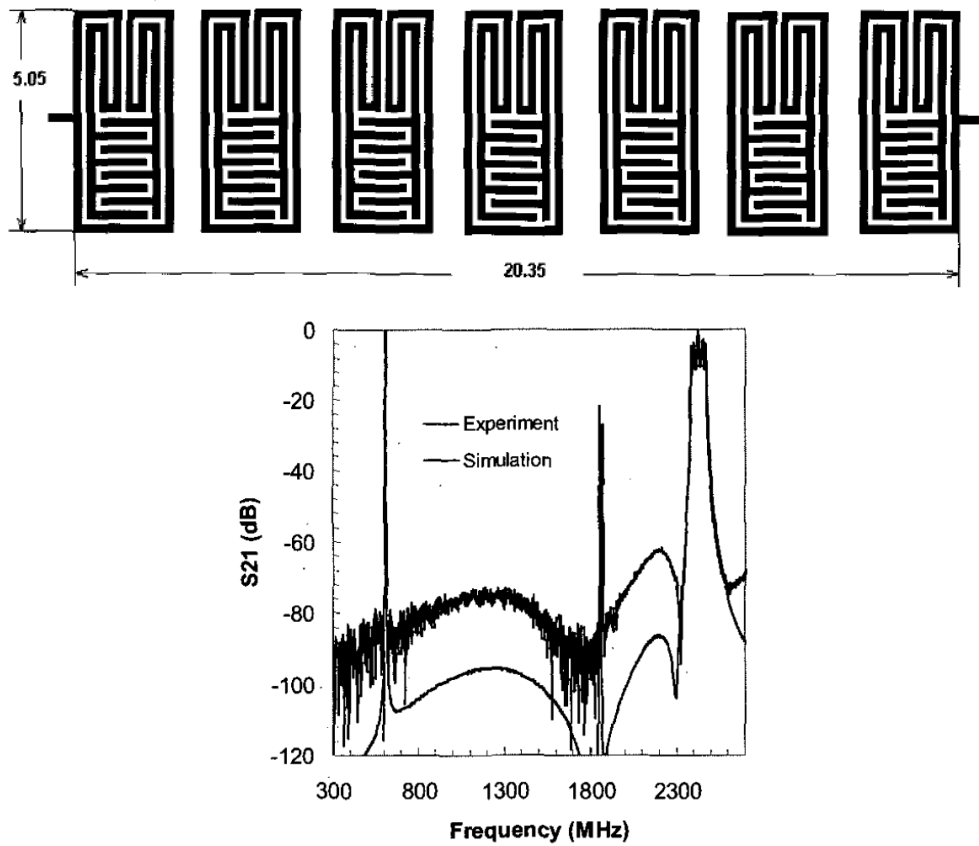


Fig. 2.3 - 10. Layout of a seven-pole filter using the resonator shown in Fig. 2.3 -9 (Dimensions are in millimeters), and its wide-range simulated and measured results. [13]

Figure 2.2-2 illustrates that the surface resistance of Nb at 70 GHz is around two to three thousand times higher than that of Nb at 1 GHz when Nb is cooled down to 7.7 K. Thus, if the filter proposed in [13] is designed at 70 GHz, the  $Q$  value of the resonator will deteriorate below 100. The double-spiral inductors can also be realized by using slot transmission lines. In [14], high- $Q$  double-spiral slot-line resonator filters (Fig. 2.3-11) were reported. As shown in [14], the double-spiral slot-line resonator has a  $Q$  value at least three times higher than the microstrip version resonator, due to lower ohmic losses. Therefore, it is possible to develop a high- $Q$  Nb-based superconductor double-spiral (spiral-in/spiral-out) inductor and interdigital capacitor resonator filter at mm-Wave frequency.

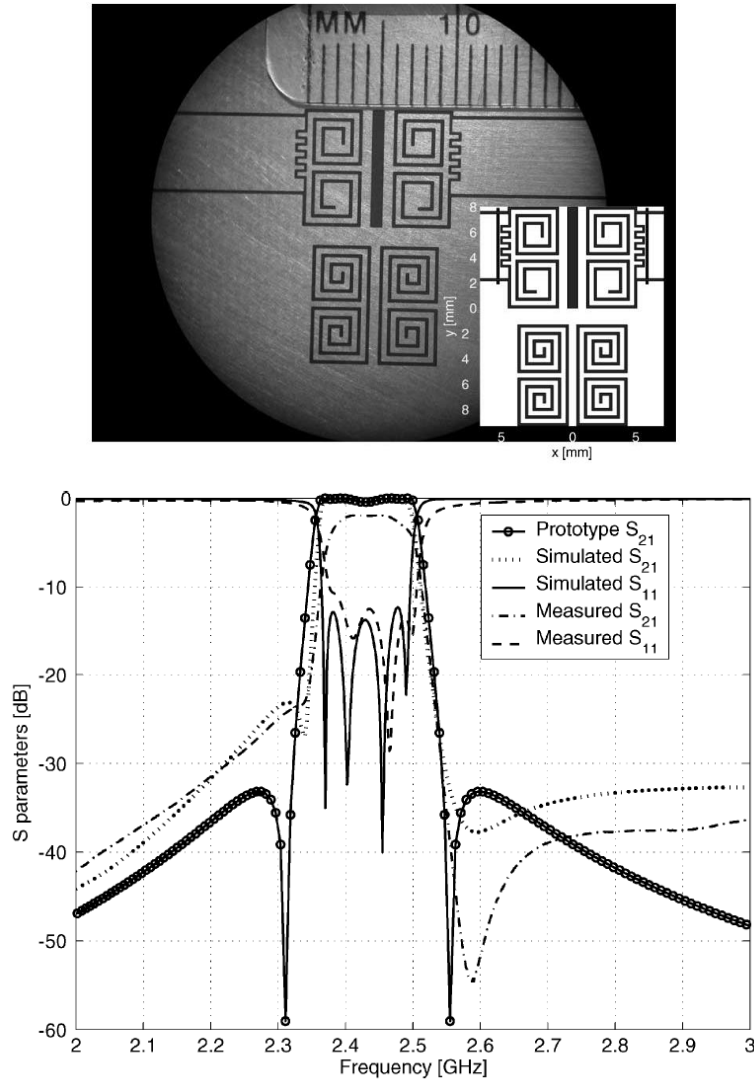


Fig. 2.3 - 11. Photograph of a miniature slot-line resonator filter and its simulated and measured results. [14]

Finally, an HTS microstrip bandpass filter with the unloaded  $Q$  value of 45,000 reported in [15] is highlighted in this section, as that study [15] focuses on the development of an ultra-narrowband filter. The proposed ultra-narrowband filter is designed at the center frequency of 4.102 GHz with a fractional bandwidth of 0.02%. Further, it is realized by depositing and patterning the YBCO thin film on a 500  $\mu\text{m}$  thick MgO wafer. The canonical coupling structure and the layout of this proposed 6-pole filter is shown in Fig. 2.3-12. As one can see from the layout, extra microstrip lines are added in between resonators 1 and 3 as well as between 4 and 6 to suppress the undesired parasitic cross-couplings between non-adjacent resonators. The extra microstrip lines can be used to produce couplings with opposite signs to the unexpected parasitic cross-couplings. This is very important for developing ultra-narrow band filters, which have a fractional bandwidth of less than 0.1%. The main couplings of the ultra-narrowband filter are very small and at the same level as the undesired parasitic cross-couplings, while the main couplings of the narrow band and wideband filter are typically at least two or three orders higher than the undesired cross-couplings.

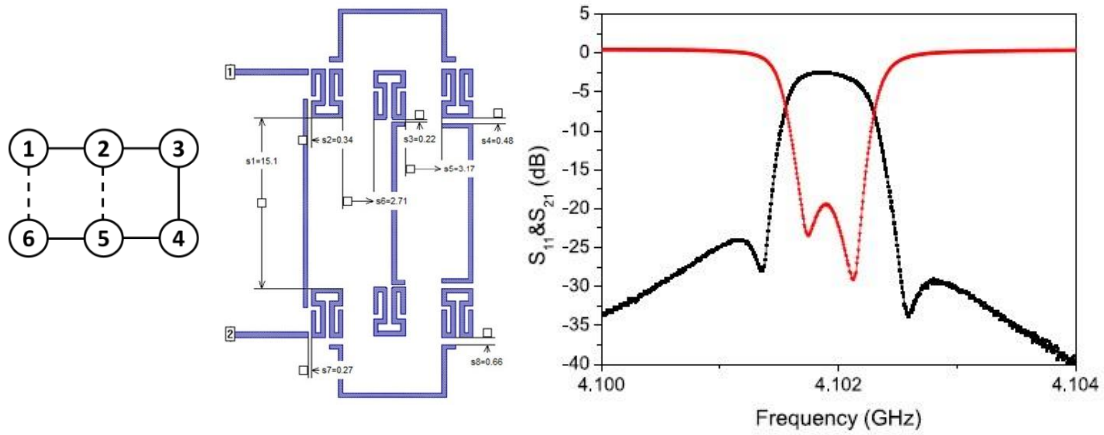


Fig. 2.3 - 12. The layout of a ultra-narrow band superconductor filer, and its measured result. [15]

## 2.4 Bulk Micromachining Filters

As shown in the previous section, superconductor filters have high- $Q$  values and compact physical sizes, but their disadvantage is that they need to be cooled down to cryogenic temperatures. Moreover, as the operating frequency increases, the surface resistance of superconductors increases dramatically. For example, as shown in Fig. 2.2-2, the surface resistance of the HTS (YBCO) is larger than that of copper at 77K when the operating frequency is above 100 GHz. For applications that do not allow for the use of superconductors, 3D resonators need to be used instead to construct high- $Q$  filters. Conventionally, 3D resonators are fabricated using computer numerical controlled (CNC) machining technologies. Advanced CNC machining techniques, such as electrical discharge machining (EDM), water-jet machining and laser-cutting machining, can be used to realize structures with the feature sizes down to few hundred micrometers.

Nevertheless, the manufacturing accuracy and tolerance of CNC machining technologies are not suitable for highly miniature filters. To compensate for manufacturing tolerance, tuning screws are required for post-fabrication. [9] However, it becomes impossible to equip filters with tuning screws when the filters have compact physical sizes. Micromachining techniques employ short wavelength lights (e.g., Ultraviolet light, X-ray, e-beams) to transfer the designed geometric patterns to a thin light-sensitive photoresist layer on the substrate. Subsequent processing steps are then used to build designed patterns on the substrate with chemical and molecule level physical treatments. Thus, micromachining techniques have much higher manufacturing accuracy and are emerging as the technology of choice for miniature high- $Q$  3D resonator filters.

Currently, several waveguide filters have been realized by using surfacing micromachining techniques [16]-[19]. However, the associated complexity, the large number of process steps, and the high prototyping cost make it difficult for surface micromachining waveguide filters to be promoted. Nowadays, with the development of silicon (Si) deep reactive ion etching (DRIE) technologies, waveguide filters with vertical sidewall on Si wafers can be realized. Next in this section, the working principles of DRIE technologies and several highlighted Si-based micromachining waveguide filters are reviewed.

DRIE is a highly anisotropic etching process developed to create high aspect ratio trenches on Si wafers for microelectromechanical system (MEMS) applications. Compared to other etching technologies (Fig. 2.4-1), the most attractive feature of DRIE for RF filter designers is the ability to create nearly vertical side walls of the etched structures, which makes it feasible to realize



waveguide resonators with Si wafers. Currently, there are two well-known DRIE processes: the Bosch process and the Cryogenic process.

The Bosch process was developed by the German company Robert Bosch GmH. Figure 2.4-2 shows the working principles of the process. The mask is coated on the Si wafer first, and the area needed to be etched is uncovered. Octafluorocyclobutane ( $C_4F_8$ ) gas is typically used to create the passivation film.

As presented in Fig. 2.4-3, the  $C_4F_8$  molecule is ring-shaped in the gas state. In the plasma state, the ring shaped  $C_4F_8$  gas molecule is broken and becomes a chain-shaped molecule with two active ends. The chain-shaped molecule then joins with other chain-shaped molecules, leading to a

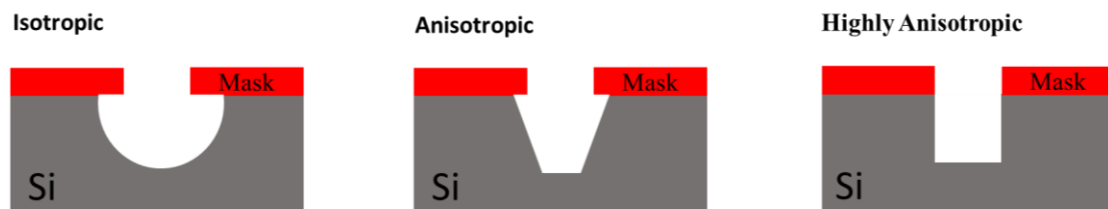


Fig. 2.4 - 1. The isotropic etching, the anisotropic etching, and the highly anisotropic etching.

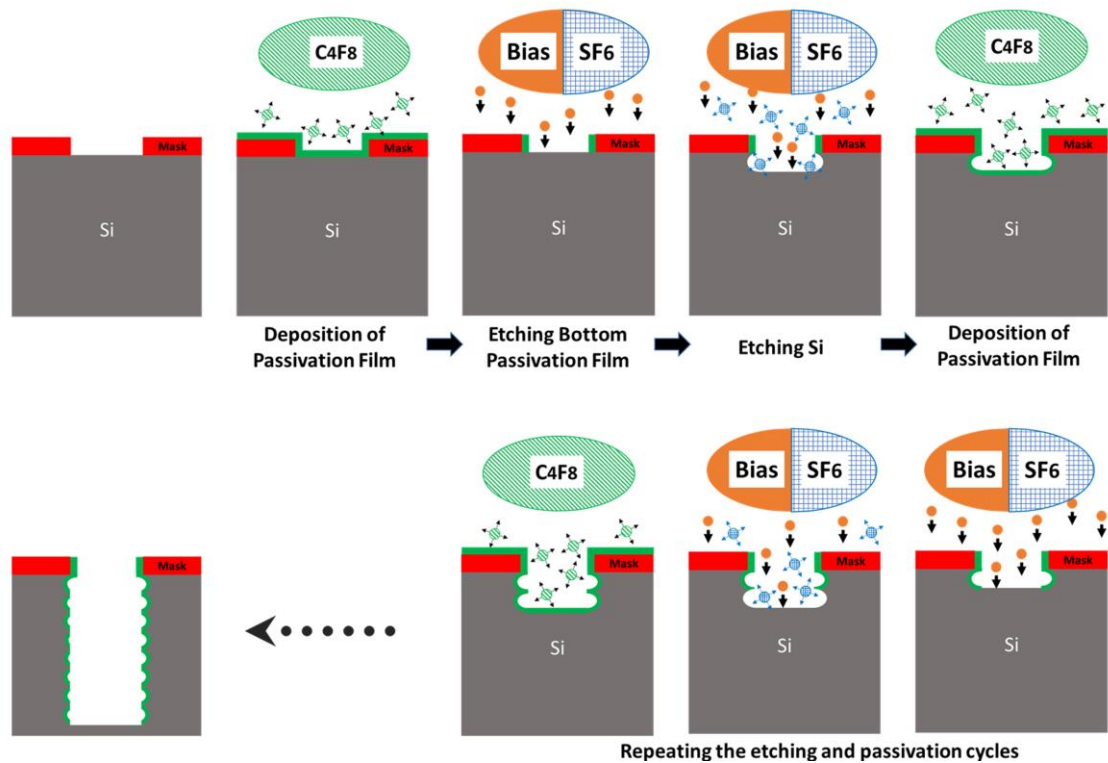


Fig. 2.4 - 2. The Bosch DRIE process. [20]-[22]

formation of the  $C_4F_8$  film layer on the wafer. Once the passivation film is created, the injection of  $C_4F_8$  gas is paused. Next, sulfur hexafluoride ( $SF_6$ ) gas is injected into the vacuumed processing chamber and dissociates in plasma to form positive ions ( $SF_4^+$  or  $SF_2^+$ ) and atomic fluorine. The positive ions are accelerated by the bias voltage and bombard the upward-facing parts of the passivation film from a nearly vertical direction, etching them away. After breaking through the upward-facing passivation film, atomic fluorine reacts with the Si as chemical etching (isotropic), with silicon tetrafluoride ( $SiF_4$ ) gas being the product of the chemical etching. During the etching cycle, the remaining passivation layer on the sidewalls protect the Si from being etched further laterally, because the accelerated ions bombard the wafer from a nearly vertical direction and  $C_4F_8$  does not react with  $SF_4$  and F. The passivation and etching cycles are repeated alternatively until structures with nearly vertical sidewalls are realized on the Si wafer [20]-[22].

The cryogenic process requires an operating temperature of  $-110\text{ }^\circ\text{C}$ . This ultra-low temperature is used to slow down the chemical isotropic etching reaction, leaving physical etching as the primary etching mechanism. There are two main drawbacks that make the cryogenic process incompatible with most applications. First, the physical etching process generates a significant amount of particles that have a tendency to directly redeposit on the wafer. This issue is more pronounced for long-term etching processes. The other main issue with the cryogenic process is that most masks will crack at this low temperature. For these reasons, the Bosch process is the more recognized DRIE production technique.

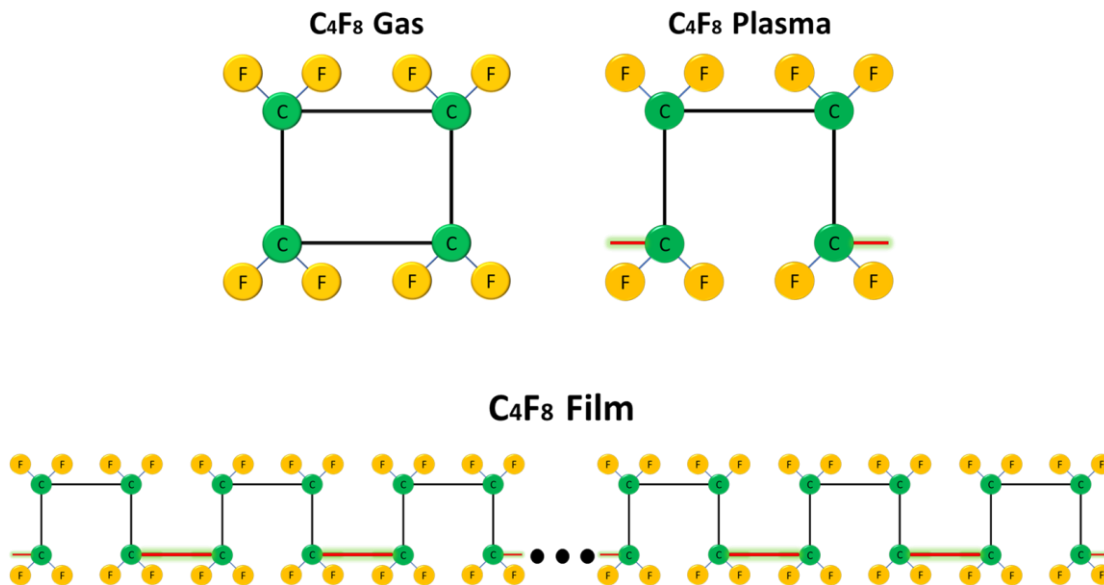


Fig. 2.4 - 3. The Octafluorocyclobutane ( $C_4F_8$ ) molecule in plasma has two active ends which allows to form a thin film. [20]-[22]

The mm-Wave filter reported in [23] is a good example of an Si-based bulk micromachining air-cavity resonator filter. As shown in Fig. 2.4-4, the proposed air-cavity resonator consists of two parts. The top air-cavity structure is realized by etching the Si wafer using the DRIE process; the bottom substrate is developed with surface micromachining techniques to construct the lid of the cavity. Then, the air-cavity resonator is acquired by joining the two developed substrates using the flip-chip technique. A four-pole bandpass filter designed at the center frequency of 93.7 GHz with a 3-dB fraction bandwidth of 3% is fabricated and tested. The measurement results shown in Fig. 2.4-5 exhibit that the fabricated filter has an unloaded  $Q$  value of 560, and that the micromachining techniques provide high manufacturing accuracy and tolerance.

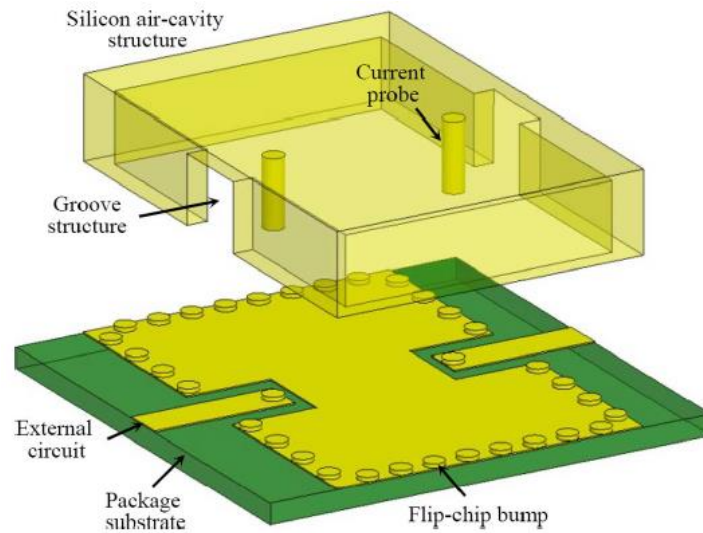


Fig. 2.4 - 4. The layer-by-layer view of a micromachine cavity resonator. [23]

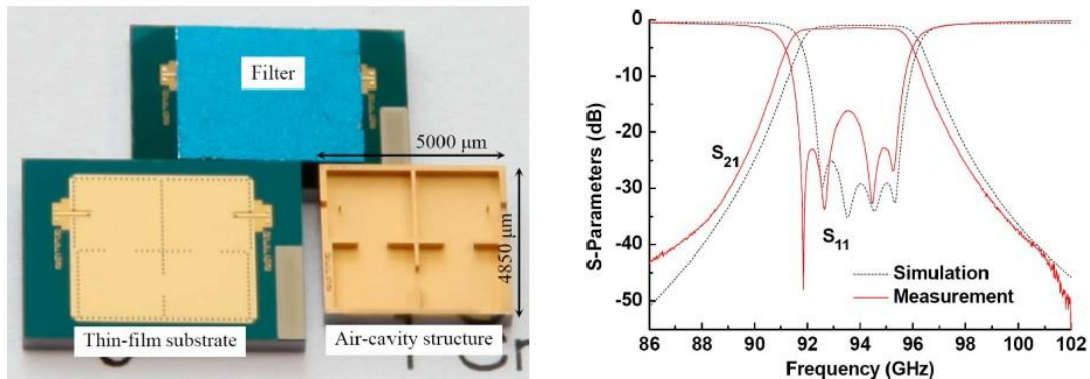


Fig. 2.4 - 5. The photograph of a fabricated micromachine cavity resonator filter, and its simulated and measured results. [23]

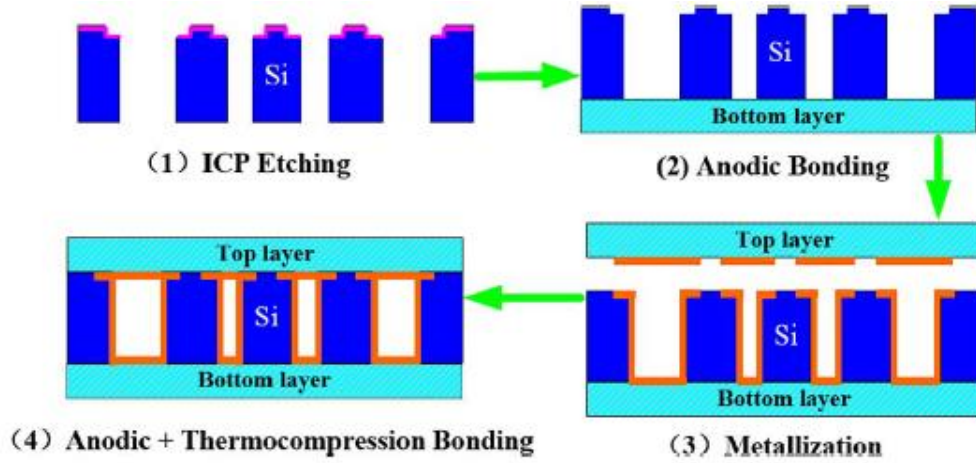


Fig. 2.4 - 6. A micromachining process can be used to fabricate cavity resonator filters. [24]

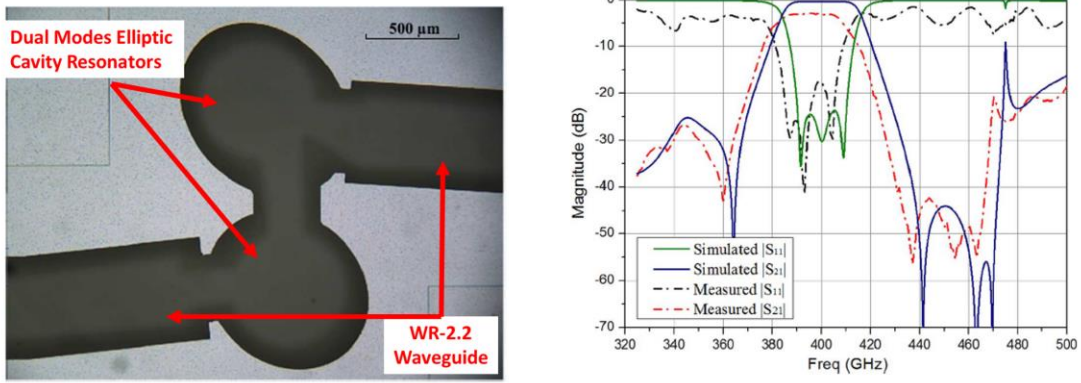


Fig. 2.4 - 7. The X-ray photograph of a fabricated micromachine dual-mode cavity resonator filter and its simulated and measured results. [24]

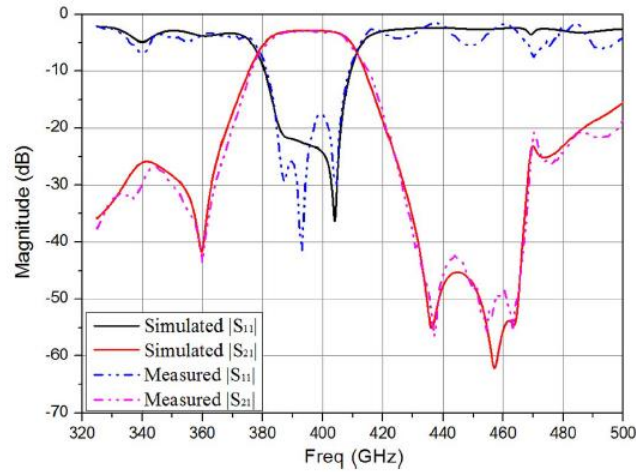


Fig. 2.4 - 8. After including the surface roughness and the non-perfect vertical cavity sidewall profile in the simulation, the simulated results match the measured results well. [24]

Due to superior manufacturing accuracy and tolerance, the DRIE technology is becoming a popular method for manufacturing high- $Q$  cavity resonator filters for THz applications. In [24], an elliptic cavity resonator filter is designed at the center frequency of 0.4 THz. A bulk micromachining process shown in Fig. 2.4-6 is used to fabricate this THz elliptic cavity resonator filter. The cavity structures are first realized by etching through an Si wafer with the DRIE technology. Then, the bottom lid of the cavity is joined with the etched Si wafer by using the anodic bonding technique, after which the metal layers are deposited on the substrates. Finally, the thermal-compression bonding technique is used to assemble the final cavity resonator filter. Figure 2.4-7 shows the X-ray photo and the measurement results of the fabricated filter. As depicted in Fig. 2.4-8, there is a slight deviation between the original simulation and the measurement results. This is because the metal surface roughness and the non-perfect vertical cavity sidewall profile were not included in the original simulation. A re-simulation with those parameters included gives a good match between the simulation and measurement results.

Figure 2.4-9 shows a schematic view of an Si-based bulk micromachining multilayer dual-mode resonator filter designed at 270 GHz. In Fig. 2.4-10, the cavity structures are etched on different Si wafers and the final filter is assembled by stacking several of these wafers. The DRIE process is ideally designed to produce perfectly vertical sidewalls, whereas in practice the sidewalls are often slightly tapered. This can make the fabricated filter have a slightly different responses from the simulation results. Due to the compact physical size, conventional post-fabrication tunings using screws cannot be performed. Therefore, test DRIE fabrication runs can be performed to evaluate the sidewall profile and the surface roughness. Strong agreement between the simulation and the measurement results can be obtained by taking into consideration the sidewall profile and the surface roughness in the simulations, as illustrated in Fig. 2.4-11.

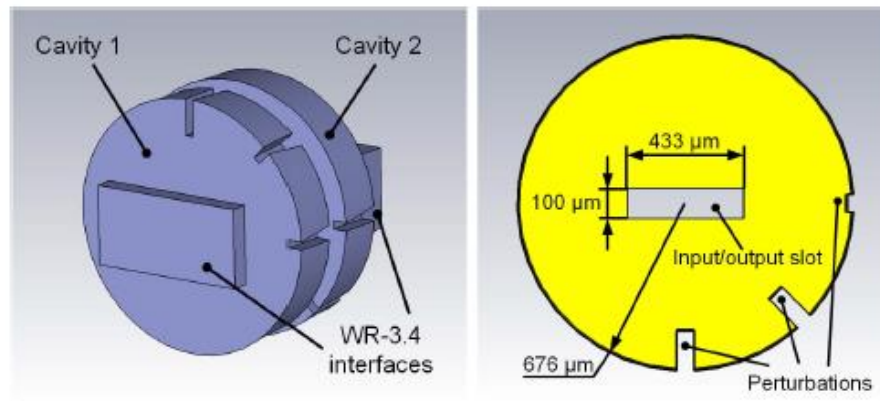


Fig. 2.4 - 9. The 3D layout of a fourth-order dual-mode cavities filter and the transversal cross-section view of a single cavity. [25]



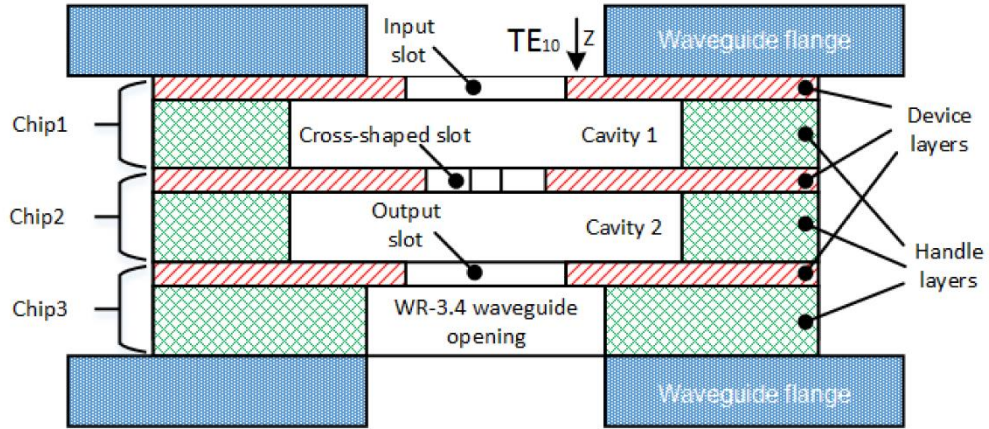


Fig. 2.4 - 10. Longitudinal cross-section view of the proposed 3-layer micromachined filter axially inserted between two waveguide flanges. [25]

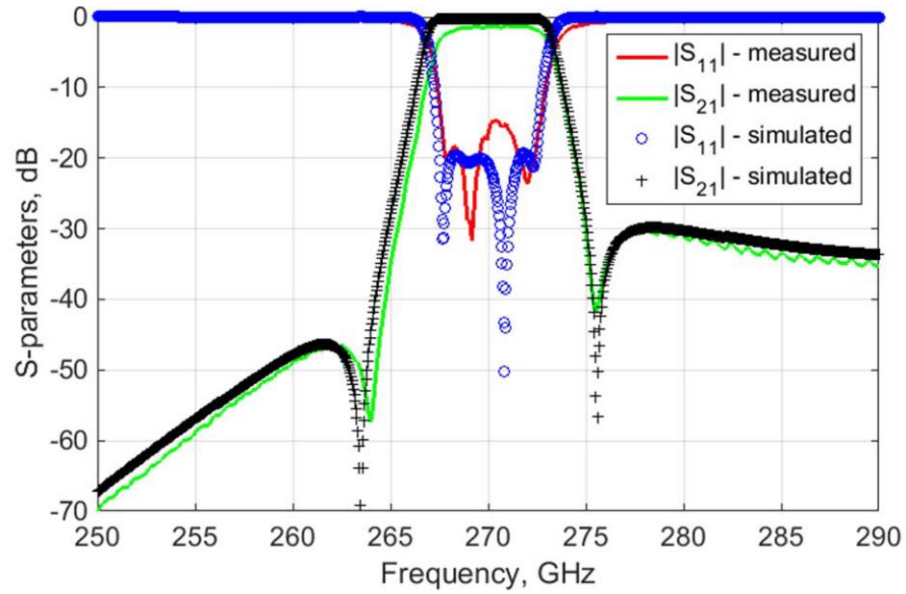


Fig. 2.4 - 11. The measured and simulated results showing excellent agreement. [25]

# Chapter 3

## An Efficient Technique for Design and Tuning of Filters and Diplexers

The design process of an RF filter can be summarized into five steps:

- 1) Synthesis of a circuit model of the filter.
- 2) Mapping the circuit model into the physical dimensions of the filter using EM simulation.
- 3) Final design optimization for the filter physical dimensions.
- 4) Fabrication.
- 5) Post-fabrication tuning the filter (optional).

To design a filter, the circuit model of the filter needs to be constructed first to meet the design specifications. Fundamental theories and methods to synthesize the filter circuit models have been well established and covered in many textbooks [9] and [26]. Conventionally, each element in the circuit model is mapped into its corresponding physical part respectively, and all the physical parts are then joint together to obtain the physical filter structure. In practice, a deviation between the responses of the circuit filter model (obtained from the Step 1) and the physical filter model (obtained from the Step 2) are always observed. This is mainly attributed to the following factors: a.) the use of frequency-independent circuit elements in the circuit filter model, while the physical elements are frequency-dependent; b.) the loading effects between the adjacent resonators are ignored in the mapping process; and c.) the unexpected parasitic cross-couplings between nonadjacent resonator in the physical filter structure are ignored while synthesizing the circuit filter model. Consequently, it is necessary to apply final optimizations for the dimensions of the physical filter model. The final EM-based optimization requires a large amount of computational recourse and time. Particularly, the efficiency of the final EM-based optimization degrades dramatically when the complexity of the physical filter structures. Various techniques, such as the space-mapping technique [27], the vector fitting technique [28] and the fuzzy logical technique [29], have been employed to improve the efficiency of the optimization process in Step 3. Yet, those techniques could fail, especially when the deviation between the responses of the circuit filter model and the physical filter model is large. In this chapter, a novel technique for filter design and tuning

technique is introduced. By using this proposed technique, the consistency between the responses of the circuit filter model and the physical filter model is greatly improved, because the loading effects and the parasitic couplings are dealt with during the design process.

### 3.1 Introduction

As a two-port network, a microwave filter can be developed by using information from the reflection coefficient,  $S_{11}$ . In [30], A. E. Atia and A. E. Williams used the phase of  $S_{11}$  to find the poles and zeros of the input impedance ( $Z_{in}$ ), from which the inter-resonator couplings can be determined. Based on this technique, M. H. Chen introduced a sequential filter tuning method in [31]. Later, a computer aided filter tuning technique was demonstrated in [32]. To avoid the challenges of using the phase of  $S_{11}$ , J. B. Ness [33] introduced a sequential method by employing the reflected group delay (RGD) as the design parameter. With further developments, the RGD sequential method has been widely adopted for EM-based design of filters [34] - [37].

In this section, the phase information of  $Z_{in}$  is used directly as the design parameters. Unlike the group delay of  $S_{11}$ , the phase of  $Z_{in}$  has well-defined transitions that make it very easy for the designer to deal with. Fig. 3.1-1 illustrates the phase of  $Z_{in}$  of the coupled resonators, showing it has only two values (i.e.,  $\pm 90^\circ$ ) with well-defined transitions. As shown later in this chapter, the locations of these phase transitions on the frequency axis correspond to the zeros and poles of  $Z_{in}$ . Thus, only the locations of the phase transitions on the frequency axis need to be matched, while the entire RGD responses are usually required to be matched over the operating frequency band.

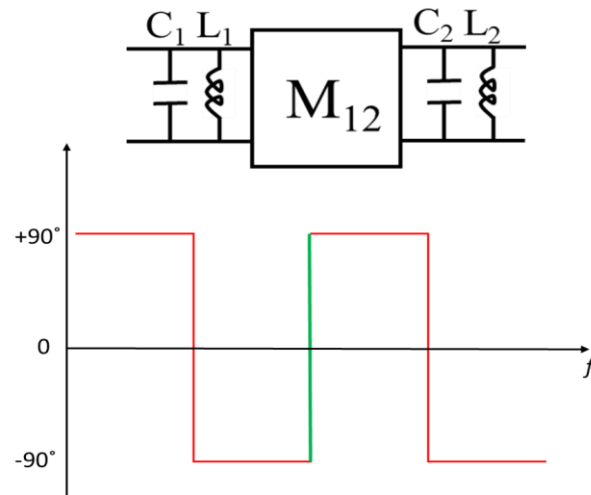


Fig. 3.1 - 1. Two ideal shunt parallel LC resonators.



Using the RGD method to tune a fabricated filter manually is relatively straightforward, but it can be quite challenging computationally for EM simulations. This is because the RGD responses need to be matched over the whole frequency band. The RGD could also become quite difficult to match, since the peaks and valleys of the RGD response may vanish when dealing with wideband high-order filters. Thus, using the phase of  $Z_{in}$  can provide a good approach for avoiding these problems.

In this chapter, we present the following:

- i) Analytical expressions for the exact frequencies of the phase transitions of the input impedance in terms of the filter coupling matrix elements are derived. By using these formulae, distinguished information about the offset in resonant frequencies and the offset in inter-resonator couplings can be easily identified. Consequently, the computation time is greatly reduced.
- ii) Since the coupling matrix model is only valid for narrowband applications, we demonstrate how the approach can be used to tune/design wideband filters using circuit models that take dispersion into considerations.
- iii) This section addresses the issue of input/output phase offset in practical filters and how it can be taken into consideration in the tuning process. It is critically important to take the phase offset into consideration, since most filter structures exhibit non-ideal input and output (I/O) ports.
- iv) We demonstrate how the concept can be applied to both Chebyshev filters and filters with transmission zeros. A wideband 5-pole CPW bandpass filter and a 4-2 combline elliptic bandpass filter are designed, fabricated, and tested.
- v) We demonstrate how the concept can be extended to design/tune diplexers.
- vi) Finally, we address the impact of the filter  $Q$  on the accuracy of the proposed PII technique, showing that using the derivative of the phase of the input impedance can help to circumvent the impact of low  $Q$  values.

## 3.2 Design Theory

The input impedance can be calculated from the lowpass prototype filter. A transfer to the bandpass filter is then employed by using the standard lowpass-to-bandpass transformation.

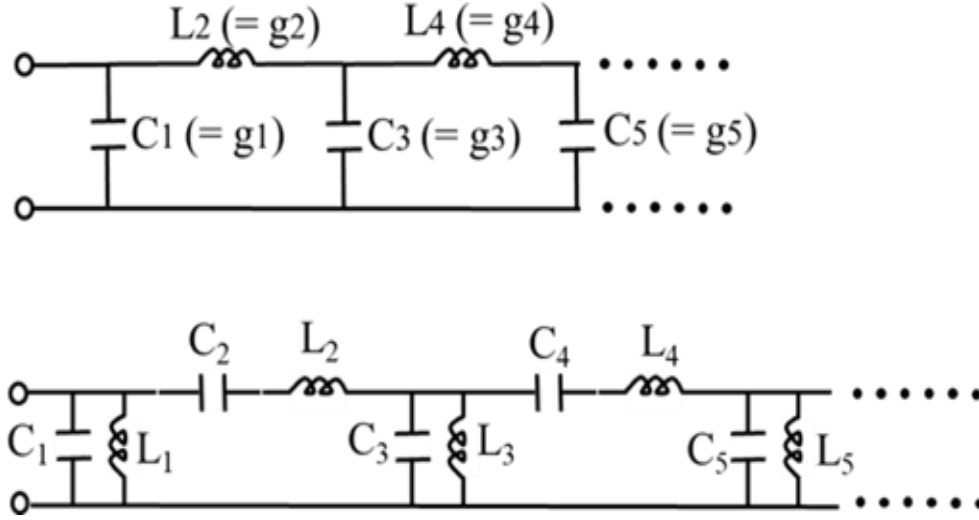


Fig. 3.2 - 1. Lowpass prototype network and bandpass filter.

In using the sequential tuning technique at the 1<sup>st</sup> stage, there is only one shunt capacitor in the lowpass filter, as shown in Fig. 3.2-1. Its input impedance is:

$$Z_{in_{lowpass}} = -j \frac{1}{\omega' g_1}, \quad (3.1)$$

where  $\omega'$  is the angular frequency of the lowpass prototype and  $g_1$  is the lowpass prototype value. The input impedance of the bandpass filter can then be obtained by using the standard lowpass-to-bandpass transformation:

$$\omega' \rightarrow \frac{\omega_0}{BW} \left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right), \quad (3.2)$$

where  $\omega$  is the angular frequency of the bandpass filter, and  $BW$  and  $\omega_0$  are the bandwidth and the center frequency of the bandpass filter. The 1<sup>st</sup> stage input impedance of the bandpass filter in Fig. 3.2-1 can thus be expressed as:

$$Z_{IN}(\omega) = -j \frac{BW g_1 \omega}{\omega^2 - \omega_0^2}. \quad (3.3)$$

As can be seen, the phase of  $Z_{in}$  is  $+90^\circ$  when  $\omega < \omega_0$  and  $-90^\circ$  when  $\omega > \omega_0$ . A phase transition occurs when  $\omega = \omega_0$  and  $Z_{in}$  is infinity.

Similarly, the 2<sup>nd</sup> stage input impedance of the bandpass filter can be obtained as:

$$Z_{IN}(\omega) = -j \frac{BW g_2 \omega^3 - BW g_2 \omega \omega_0^2}{g_1 g_2 \omega^4 + g_1 g_2 \omega_0^4 - BW^2 \omega^2 - 2 g_1 g_2 \omega^2 \omega_0^2}. \quad (3.4)$$

By solving the numerator and denominator, respectively, the locations of the 2<sup>nd</sup> stage phase transitions on the frequency axis can be obtained as follows:

$$\omega_1 = \omega_0, \quad (3.5)$$

$$\omega_2 = \frac{\sqrt{\frac{BW^2}{g_1 g_2} + 4\omega_0^2} - \frac{BW}{\sqrt{g_1 g_2}}}{2}, \quad (3.6)$$

$$\omega_3 = \frac{\sqrt{\frac{BW^2}{g_1 g_2} + 4\omega_0^2} + \frac{BW}{\sqrt{g_1 g_2}}}{2}. \quad (3.7)$$

The inter-resonator coupling can be expressed as:

$$M_{i,i+1} = \frac{1}{\sqrt{g_i g_{i+1}}}, \quad (3.8)$$

where  $i=1, 2, 3, \dots$ . Consequently, equations (6) and (7) can be written in terms of the filter coupling matrix element  $M_{ij}$  as:

$$\omega_2 = \frac{\sqrt{M_{12}^2 + 4\frac{1}{\Delta^2}} - M_{12}}{2(\Delta\omega_0)^{-1}}, \quad (3.9)$$

$$\omega_3 = \frac{\sqrt{M_{12}^2 + 4\frac{1}{\Delta^2}} + M_{12}}{2(\Delta\omega_0)^{-1}}, \quad (3.10)$$

where  $\Delta$  is the fractional bandwidth of the bandpass filter.

Equations (3.5), (3.9) and (3.10) show that the middle phase transition locates at  $\omega_0$  and is not affected by the inter-resonator coupling  $M_{12}$ . Varying  $M_{12}$  only affects the locations of the side phase transitions. Analogously, the phase transition locations for the successive stages can be calculated.

Equations in the Table 3.1 give the third and fourth stages' phase transitions locations of the bandpass filter in terms of the inter-resonator couplings,  $M_{i,i+1}$ . In reviewing the expressions of the phase transition locations, it is easy to see that the location of the middle phase transition is always at  $\omega_0$ . Once the phase transition locations of each stage are acquired, the inter-resonator couplings,  $M_{i,i+1}$ , can be mapped into the physical dimensions of the filter, and the physical realization of the bandpass filter can be developed by matching the phase of the input impedance (PII) responses stage by stage.

It should be noted that the 1<sup>st</sup> stage PII response has only one phase transition, which only contains the information of the 1<sup>st</sup> resonator's resonant frequency,  $f_{R1}$ . Thus, at the 1<sup>st</sup> stage, the input coupling of the bandpass filter can be mapped into physical dimensions by using other conventional methods, such as the techniques described in [9] and [26]. Once the input coupling and  $f_{R1}$  of the physical realization of the bandpass filter are well-tuned, the 2<sup>nd</sup> resonator is added to the design circuit. Then,  $M_{12}$  and  $f_{R2}$  of the physical realization of the bandpass filter need to be tuned at the 2<sup>nd</sup> stage.

As mentioned previously,  $M_{12}$  does not affect the location of the middle phase transition. Therefore,  $f_{R2}$  of the physical realization of the bandpass filter is adjusted first to make the middle phase transition occur at  $\omega_0$ . Next,  $M_{12}$  of the physical realization of the bandpass filter is adjusted to match the required 2<sup>nd</sup> stage PII response. At the 3<sup>rd</sup> stage, the 3<sup>rd</sup> resonator is added to the design circuit. Similarly,  $f_{R3}$  is adjusted first to ensure that the middle phase transition occurs at  $\omega_0$ . Since  $f_{R1}$ ,  $f_{R2}$ ,  $M_{12}$  and the input coupling of the physical realization of the bandpass filter are already well-tuned at the previous stages, only  $M_{23}$  of the physical realization of the bandpass filter needs to be adjusted to match the required 3<sup>rd</sup> stage PII response. The steps are then repeated until all the resonators and inter-resonator couplings are well-tuned.

### 3.3 Application of PII Technique to Narrowband Filters

In order to clearly demonstrate the working principle of the proposed method, a 3-pole narrowband microstrip Chebyshev filter with a fractional bandwidth of 1% is designed step by step in this section. The filter, as shown in Fig. 3.3-1, is designed on a 635  $\mu\text{m}$  Alumina with a loss tangent of 0.0002. A lossless metal is assumed for the conductor. A coupling matrix with a return loss of 25 dB is used as the reference circuit model, and the EM model is built using Sonnet<sup>®</sup>.

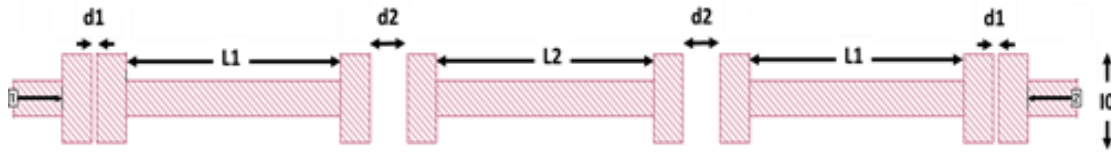


Fig. 3.3 - 1. Physical layout of three-pole narrowband Chebyshev filter.

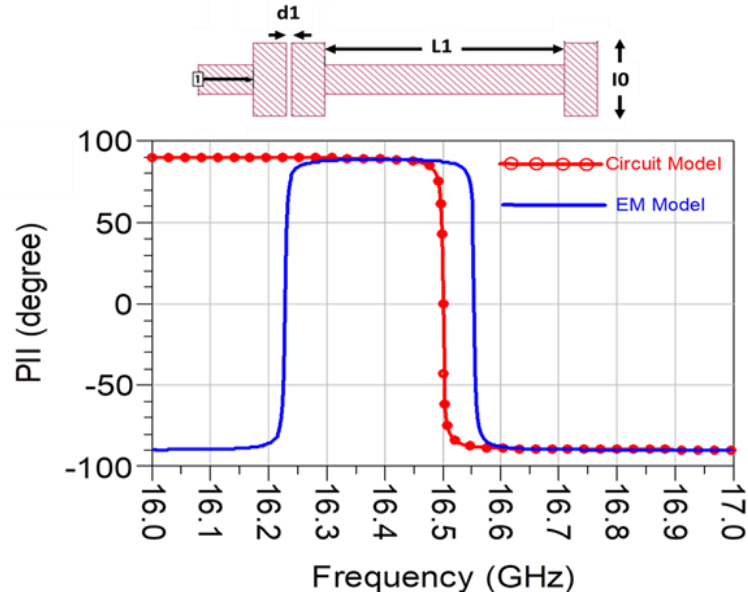


Fig. 3.3 - 2. The 1<sup>st</sup> stage physical layout and PII responses.

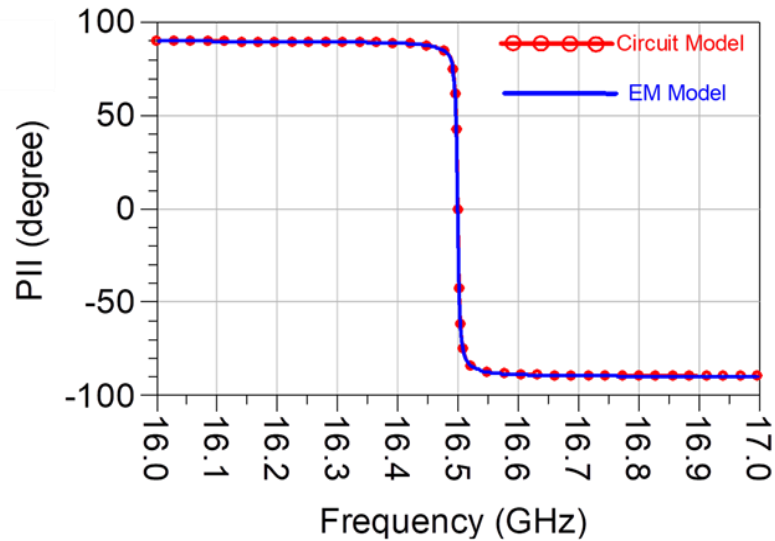


Fig. 3.3 - 3. The 1<sup>st</sup> PII response after the unknown transition line is removed:  $d1 = 0.009$  mm;  $L1 = 4.375$  mm;  $l0 = 1.5$  mm.

Fig. 3.3-2 shows the phase of the input impedance of the 1<sup>st</sup> stage, calculated using the coupling matrix circuit and EM models. As can be seen from Fig. 3.3-2, the two PII responses are not matched and the PII response of the EM model has two phase transitions. From the analysis provided in Section 3.2, the 1<sup>st</sup> stage PII response should have only one phase transition. The reason of having the extra phase transition in the PII response of the EM model is that the input reference plane of EM model is not exactly the ideal port of the input inverter in the circuit model. Thus, an unexpected unknown phase offset is introduced between the physical reference plane and the port

of the corresponding inverter in the circuit model. Therefore, such phase offset needs to be removed from the EM simulation result. In order to extract the equivalent transmission line that represents the phase offset, one can use the methods reported in [31] and [38].

In this chapter, the equivalent electrical length of the unknown transmission line is extracted using a different method, which is outlined in Section 3.5. Once the equivalent electrical length is extracted, it can be de-embedded from the EM simulation leading to the PII response shown in Fig. 3.3-3.

At the 2<sup>nd</sup> stage, the second resonator is added to the EM circuit, as shown in Fig. 3.3-4. The initial value for  $L2$  is selected to be equal to  $L1$ , and  $d2$  is selected to be 650  $\mu\text{m}$  as the initial value for further tuning. Fig. 3.3-5 shows both the RGD response and the PII response of the 2<sup>nd</sup> stage with the initial values set for  $L2$  and  $d2$ .

Optimizing  $L2$  and  $d2$  manually so that the RGD response (Fig. 3.3-5a) of the EM model matches that of the circuit model is often quite challenging. Traditionally, a space-mapping technique needs to be used to obtain a good match between the two RGD responses with a minimum number of EM

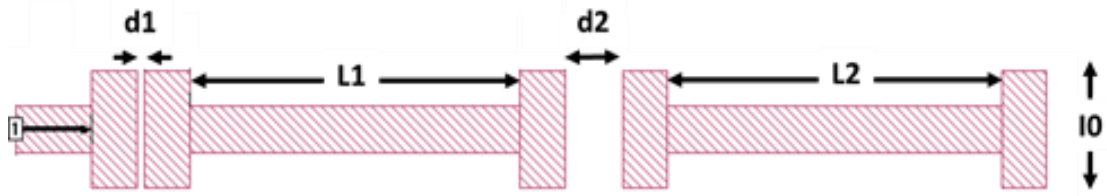


Fig. 3.3 - 4. The 2<sup>nd</sup> stage physical layout.

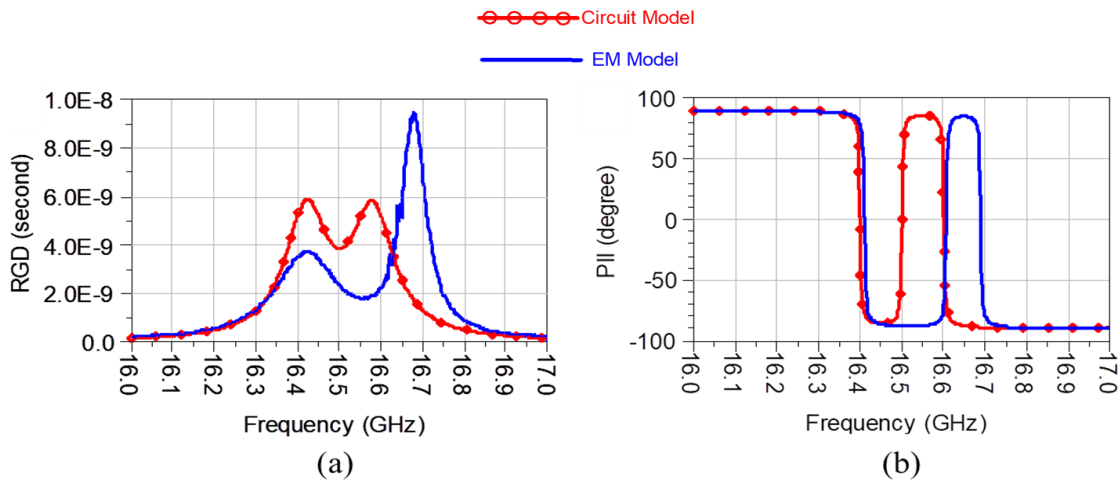


Fig. 3.3 - 5. The 2<sup>nd</sup> stage RGD responses and PII responses:  $d1 = 0.09 \text{ mm}$ ;  $d2 = 650 \text{ mm}$ ;  $L1 = L2 = 4.375 \text{ mm}$ ;  $h = 1.5 \text{ mm}$ .

simulations, as demonstrated in [35] and [39]. This issue becomes more pronounced when dealing with large-order filters, when the EM model RGD with 3 or 4 resonators needs to be matched to that of the circuit mode. On the other hand, the use of the PII response significantly simplifies the

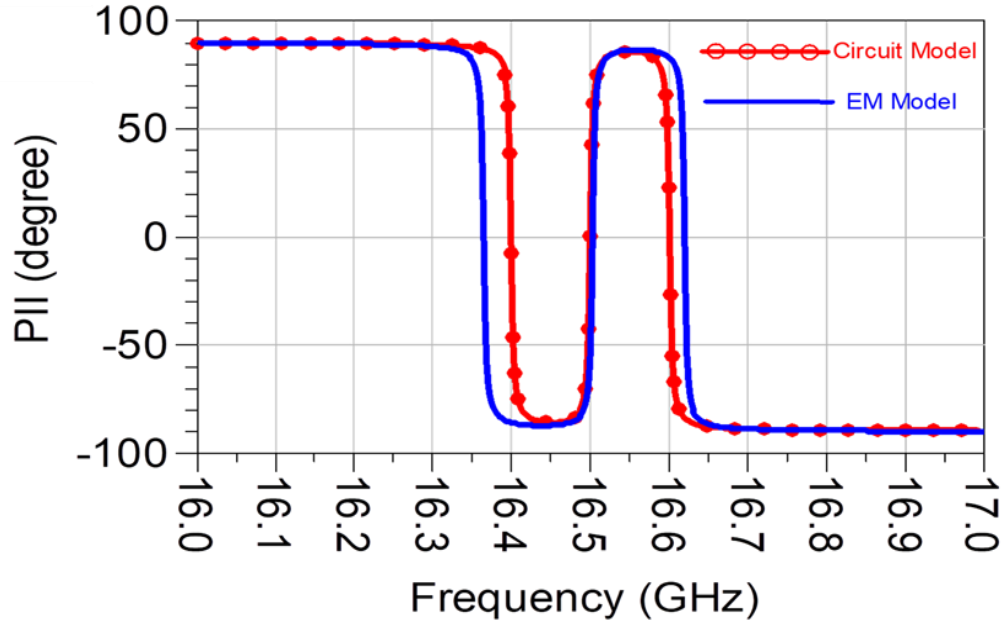


Fig. 3.3 - 6. The 2<sup>nd</sup> stage PII responses:  $d1 = 0.09$  mm;  $d2 = 0.65$  mm;  $L1 = 4.375$  mm;  $L2 = 4.415$  mm;  $l0 = 1.5$  mm.

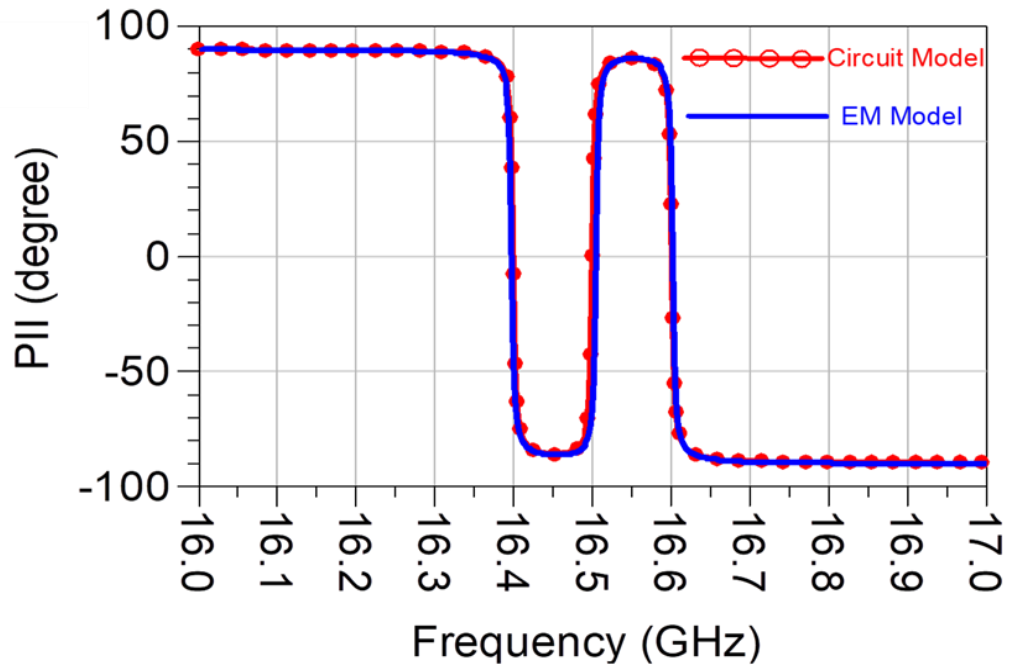


Fig. 3.3 - 7. The 2<sup>nd</sup> stage PII responses:  $d1 = 0.09$  mm;  $d2 = 0.73$  mm;  $L1 = 4.375$  mm;  $L2 = 4.415$  mm;  $l0 = 1.5$  mm.

tuning process. Fig. 3.3-5b shows the 2<sup>nd</sup> stage PII response, with the middle phase transition higher than  $\omega_0$ . As mentioned previously in Section 3.2,  $L_2$  is thus increased first to make the middle phase transmission occur at  $\omega_0$ .

Fig. 3.3-6 shows that the middle phase transition locates at  $\omega_0$  when  $L_2$  is well-tuned, and that the two side phase transitions of the EM model PII response have a wider separation than those of the reference coupling matrix circuit model. From equations (3.9) and (3.10), we can see that in order to move the phase transition at  $\omega_2$  up and the phase transition at  $\omega_3$  down in frequency,  $M_{12}$  needs to be reduced. The designer can then increase the gap  $d_2$  until the PII response of the EM model matches that of the circuit model, as shown in Fig. 3.3-7. This highlights the benefits of the equations given in Table 3.1 in guiding the designer during the optimization process.

One consideration in using this approach needs to be mentioned here is that the loading effect of the newly added resonator in the EM model. In this example, the loading effect caused by the 2<sup>nd</sup> resonator to the 1<sup>st</sup> resonator is small enough and can be neglected. Similar to all sequential design techniques (including the RGD), the resonator added in the previous stage may need to be slightly adjusted to obtain good matching that accounts for the loading effects.

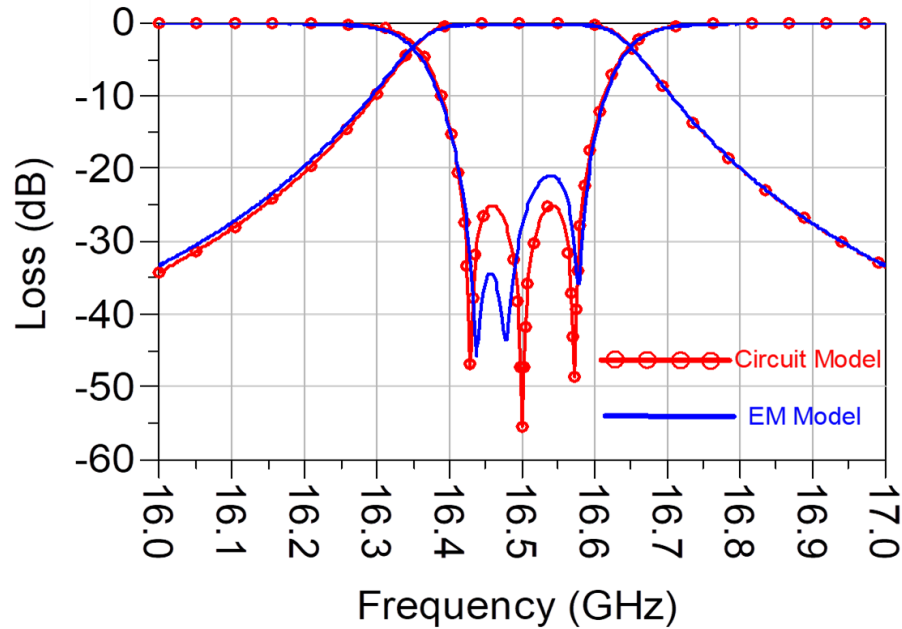


Fig. 3.3 - 8. Responses of the filter:  $d_1 = 0.09$  mm;  $d_2 = 0.73$  mm;  $L_1 = 4.375$  mm;  $L_2 = 4.415$  mm;  $l_0 = 1.5$  mm.

For a 3-pole Chebyshev filter,  $M_{S1} = M_{3L}$ ,  $M_{12} = M_{23}$  and  $f_{R1} = f_{R3}$ , and thus all the resonators and couplings are well-tuned after the 2<sup>nd</sup> stage. The final filter can be obtained by joining two halves of the filter. The final response of the 3-pole filter compared to the ideal coupling matrix circuit



response is shown in Fig. 3.3-8. As illustrated by this example, the features of the PII approach can be outlined as follows:

- a) Information about the offsets in the transitions can be related directly to resonant frequencies and inter-resonator couplings, as shown in Appendix. Thus, one can easily decide which physical dimensions need to be adjusted to obtain a good matching between the EM model and the reference circuit model, and how this adjusting should be done.
- b) The PII responses only have values of  $\pm 90^\circ$  and phase transitions, regardless of whether the inter-resonator couplings and resonant frequencies are well-tuned or not. Therefore, the main task when using the PII method to design/tune bandpass filters is matching the locations of the phase transitions to the ideal PII responses during each stage, either by using the equations given in Table I or by employing circuit simulation software, such as Keysight® ADS, to calculate the phase of the input impedance at each stage.
- c) When using the PII approach in the EM design, only the frequencies around the phase transitions of the PII response need to be simulated. This also translates to a significant reduction in the computational time needed to complete the design. Having well-defined phase transitions is a feature of the PII response that makes it very efficient for the EM design of bandpass filters.

### 3.4 Application of PII Technique to Wideband Filters

Consider the CPW wideband filter shown in Fig. 3.4-1. As can be seen, the inter-resonator couplings are realized by horizontal CPW lines tapped into the resonators to achieve high coupling values. We will first apply the PII method to tune this wideband filter using the coupling matrix model. It is well-known that the coupling matrix model cannot be used accurately for wideband

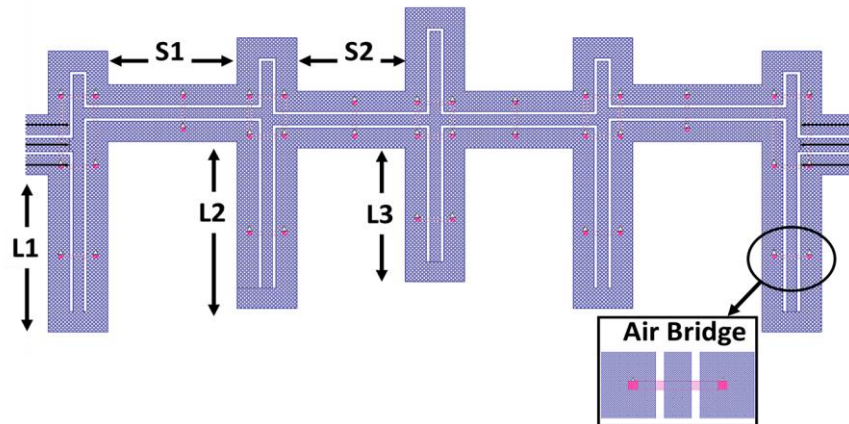


Fig. 3.4 - 1. Physical layout of CPW ultra-wideband bandpass filter design [40].

filters. However, it would be interesting to see the results achieved when using the coupling matrix model (or the equations given in Table I) for wideband filters. The same procedure used in section III is used for the wideband filter. Fig. 3.4-2 and Fig. 3.4-3 show that the PII responses of the EM wideband filter model match the ones of the coupling matrix circuit model.

Since the Chebyshev filter is physically symmetrical, after the 3<sup>rd</sup> stage, half of the resonators and couplings of the 5-pole bandpass filter are tuned. The final filter can be obtained by joining two halves of the filter. The achieved EM design as it compares to the coupling matrix circuit model is given in Fig. 3.4-4.

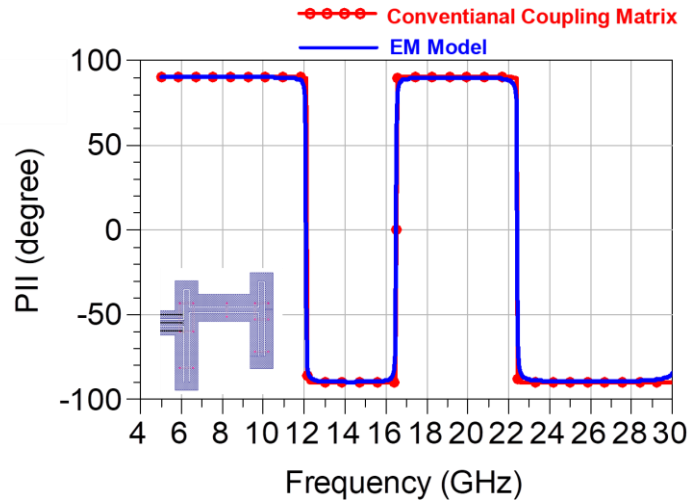


Fig. 3.4 - 2. The 2<sup>nd</sup> stage PII responses:  $L_1 = 1230 \text{ } \mu\text{m}$ ;  $L_2 = 1530 \text{ } \mu\text{m}$ ;  $L_3 = 1050 \text{ } \mu\text{m}$ ;  $S_1 = 1170 \text{ } \mu\text{m}$ ; Resonator\_1\_Length = 2430  $\mu\text{m}$ ; Resonator\_2\_Length = 2130  $\mu\text{m}$ .

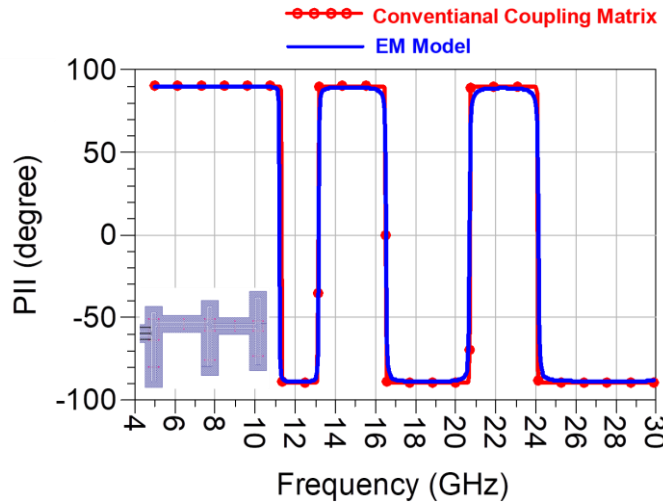


Fig. 3.4 - 3. The 3<sup>rd</sup> stage PII responses:  $L_1 = 1350 \text{ } \mu\text{m}$ ;  $L_2 = 1650 \text{ } \mu\text{m}$ ;  $L_3 = 1290 \text{ } \mu\text{m}$ ;  $L_4 = 1230 \text{ } \mu\text{m}$ ;  $L_5 = 1080 \text{ } \mu\text{m}$ ;  $S_1 = 1170 \text{ } \mu\text{m}$ ;  $S_2 = 930 \text{ } \mu\text{m}$ ; Resonator\_1\_Length = 2430  $\mu\text{m}$ ; Resonator\_2\_Length = 2250  $\mu\text{m}$ ; Resonator\_3\_Length = 2370  $\mu\text{m}$ .

The deviation between EM results and the coupling matrix circuit model is attributed to two factors: i) joining the two halves of the filter directly. Achieving a close but non-perfect match is quite common in all tuning techniques, including the RGD method and the time domain tuning technique [41]; and ii) the use of the coupling matrix mode that is limited only to narrow band applications, since it does not take the dispersion into account.

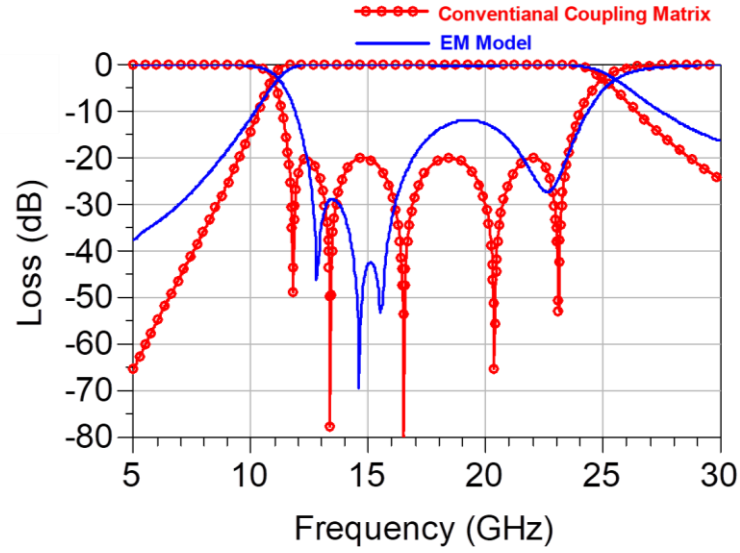


Fig. 3.4 - 4. Responses of the ultra-wideband bandpass filter without final optimization.

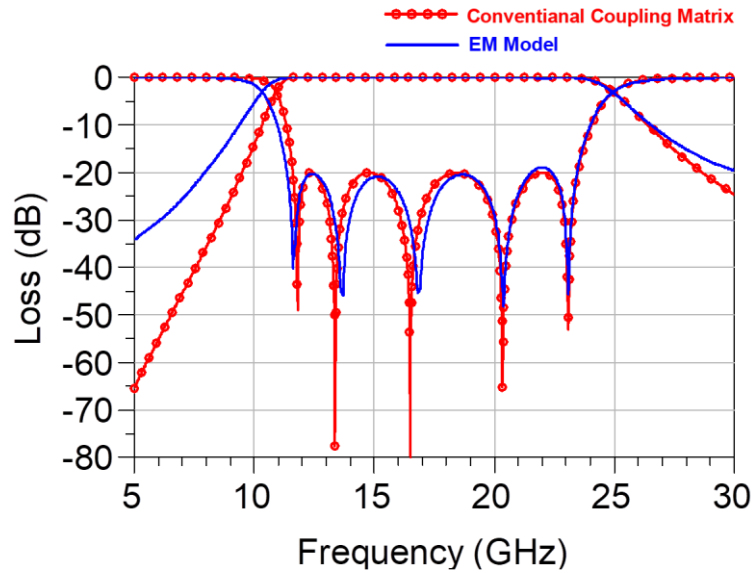


Fig. 3.4 - 5. Responses of the ultra-wideband bandpass filter without final optimization.

To isolate the impact of these two factors, the dimensions of the EM model are optimized slightly to obtain return loss below 20 dB. The results obtained are shown in Fig. 3.4-5. A noticeable deviation still exists between the  $S_{21}$  response of the designed EM model and that of the coupling matrix model. This is because the inter-resonator couplings in the conventional coupling matrix are assumed to be constant, while the inter-resonator couplings in the physical realization of the wideband bandpass filter are frequency-dependent (the dispersion effect).

The solution is to use a circuit model that is applicable to wideband filters. Over the past few years, several papers have reported on generating circuit models and coupling matrix models that are ideal for use in wideband applications [42]-[46]. We will use a circuit model based on [46], where it is shown that frequency-dependent inter-resonator couplings can be accurately modeled using the lumped LC circuit depicted in Fig. 3.4-6. Based on [46], one can use the generalized dispersive coupling (Fig. 3.4-6) to synthesize an accurate circuit model for a wideband filter, as shown in Fig. 3.4-7. A comparison between the responses of the lumped LC circuit given in Fig. 3.4-7 and the conventional coupling matrix is shown in Fig. 3.4-8. As can be seen, the frequency dependence of the coupling elements can have a very noticeable impact on the filter selectivity. The same observations are highlighted in [42]-[46].

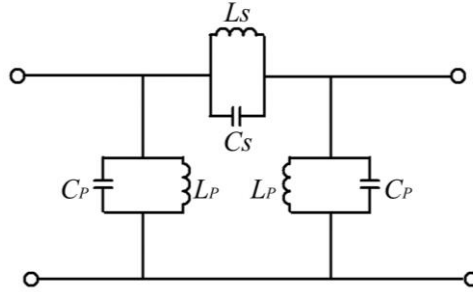


Fig. 3.4 - 6. The lumped circuit model for frequency-dependent inter-resonator coupling.

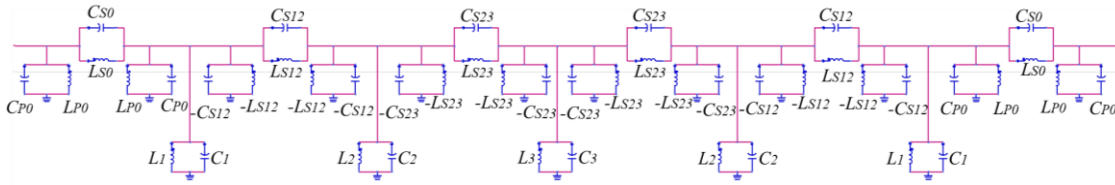


Fig. 3.4 - 7. Lumped circuit model for ultra-wideband bandpass filter with frequency-dependent inter-resonator couplings:  $C_{S12} = 0.05308 \text{ pF}$ ,  $L_{S12} = -0.81446 \text{ nH}$ ,  $C_{S23} = 0.04514 \text{ pF}$ ,  $L_{S23} = -1.19745 \text{ nH}$ ,  $C_{S0} = -37.5998 \text{ pF}$ ,  $L_{S0} = -0.47237 \text{ nH}$ ,  $C_{P0} = -2C_{S0}$ ,  $L_{P0} = -0.5L_{S0}$ ,  $L_1 = 0.32725 \text{ nH}$ ,  $C_1 = 0.25735 \text{ pF}$ ,  $L_2 = 0.30367 \text{ nH}$ ,  $C_2 = 0.28165 \text{ pF}$ ,  $L_3 = 0.33532 \text{ nH}$ ,  $C_3 = 0.26492 \text{ pF}$ .

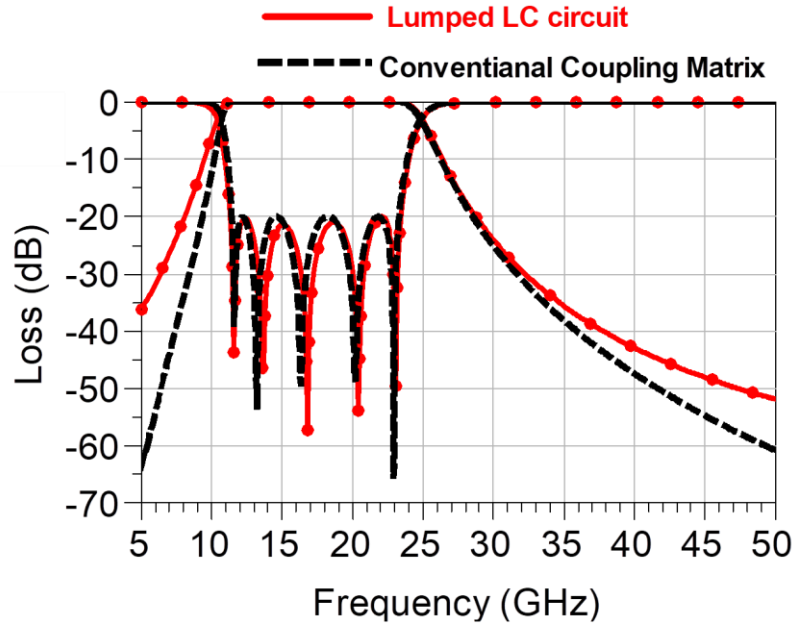


Fig. 3.4 - 8. Comparison of the lumped LC bandpass filter with conventional coupling matrix.

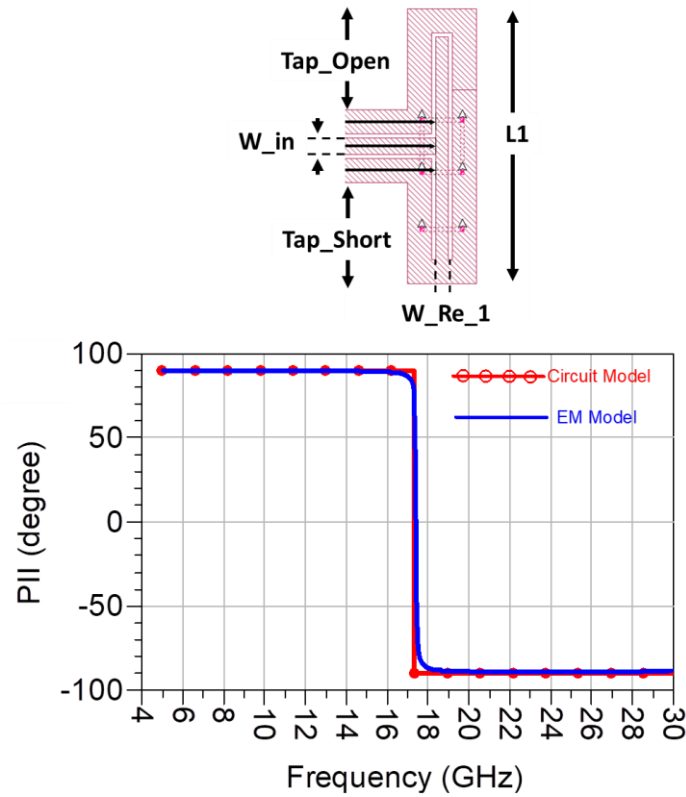


Fig. 3.4 - 9. The 1<sup>st</sup> stage PII responses:  $L1 = 2.04$  mm,  $W_{Re\_1} = 0.09$  mm,  $W_{in} = 0.12$  mm,  $Tap\_Open = 0.75$  mm,  $Tap\_Short = 0.75$  mm,  $Gap = 0.03$  mm.

Now we will apply the PII method to design the wideband filter shown in Fig. 3.4-1, using the dispersive LC circuit filter model given in Fig. 3.4-7. The first three stages PII responses and physical dimensions of the EM model filter are shown in Figs. 3.4-9 to 3.4-11.

Similarly, the physical structure in Fig. 3.4-11 is then flipped over and an EM mode filter is obtained by joining two halves of the filter in Fig. 3.4-12. Here, all the physical dimensions are obtained from the 3<sup>rd</sup> stage and no final fine-tune is applied after flipping over and joining the second half of the filter. As one can see, the EM responses generated from the PII technique closely match those of the LC circuit model. The deviation at the higher rejection band is due to the higher propagation modes in the EM model filter. As shown in this example, the proposed PII technique also works well for the design and tuning of ultra-wideband filters.

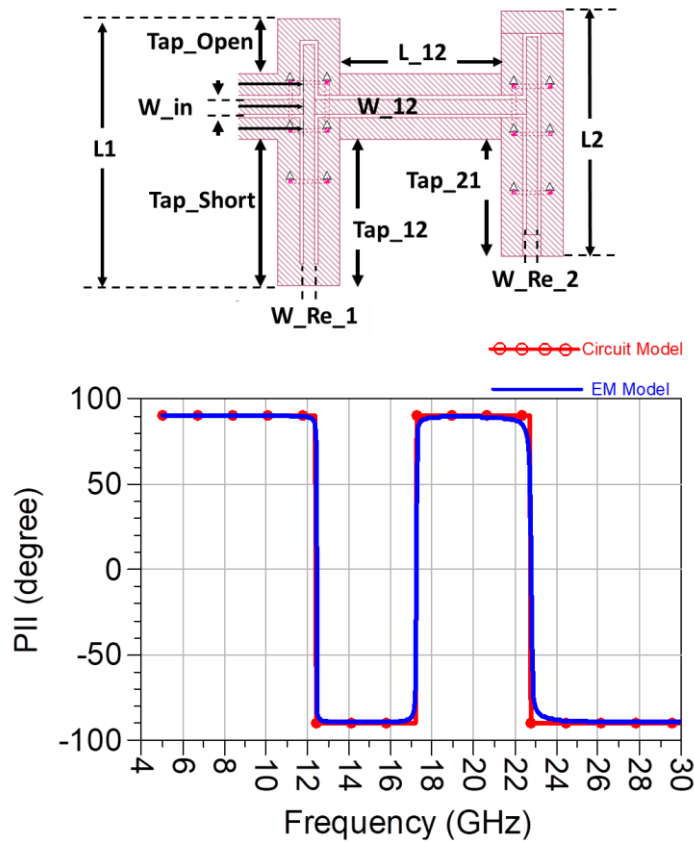


Fig. 3.4 - 10. The 2<sup>nd</sup> stage PII responses:  $L1 = 2.19$  mm,  $W_{Re\_1} = 0.09$  mm,  $W_{in} = 0.12$  mm,  $Tap\_Open = 0.45$  mm,  $Tap\_Short = 1.2$  mm,  $Gap = 0.03$  mm,  $L_{12} = 1.32$  mm,  $W_{12} = 0.12$  mm,  $L2 = 2.01$  mm,  $Tap_{12} = 1.2$  mm,  $Tap_{21} = 0.96$  mm,  $W_{Re\_2} = 0.09$  mm.

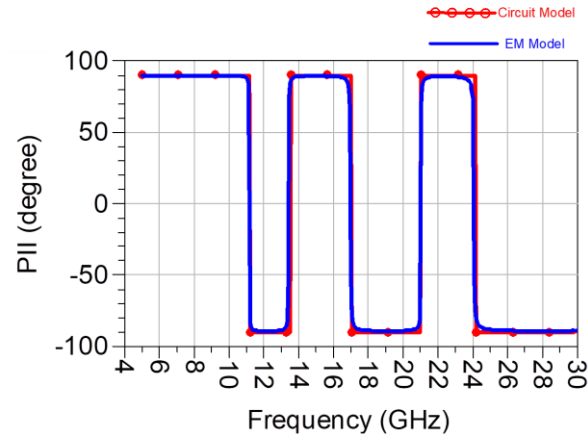
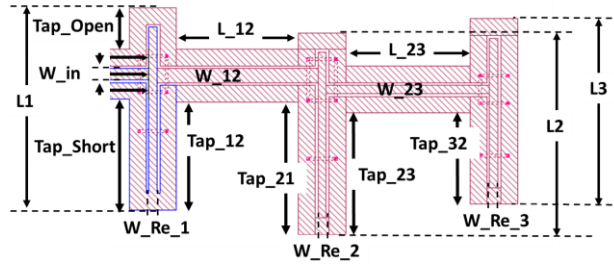


Fig. 3.4 - 11. The 3<sup>rd</sup> stage PII responses:  $L1 = 2.19$  mm,  $W_{Re\_1} = 0.09$  mm,  $W_{in} = 0.12$  mm,  $Tap\_Open = 0.45$  mm,  $Tap\_Short = 1.2$  mm,  $Gap = 0.03$  mm,  $L_{12} = 1.32$  mm,  $W_{12} = 0.15$  mm,  $L2 = 2.19$  mm,  $Tap_{12} = 1.17$  mm,  $Tap_{21} = 1.44$  mm,  $W_{Re\_2} = 0.09$  mm,  $L_{23} = 1.35$  mm,  $W_{23} = 0.09$  mm,  $L3 = 2.01$  mm,  $Tap_{23} = 1.32$  mm,  $Tap_{32} = 0.99$  mm,  $W_{Re\_3} = 0.09$  mm.

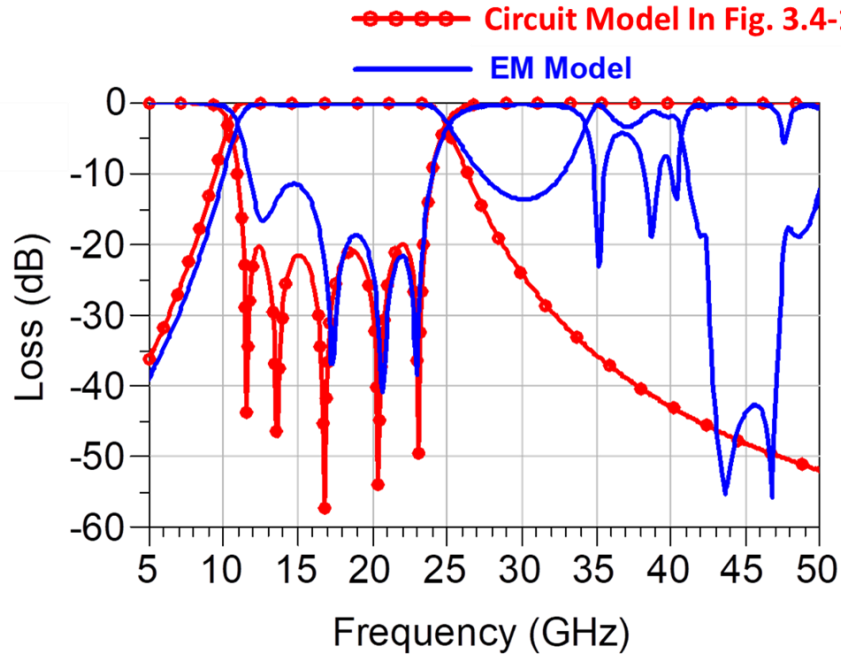


Fig. 3.4 - 12. Filter responses after the 3<sup>rd</sup> stage without final fine-tune to compensate for loading effects.

## 3.5 Application of PII Technique to Filters with Transmission Zeros

In this section, we demonstrate the application of the PII technique to filters with transmission zeros. A combline filter with two transmission zeros and a bandwidth of 90 MHz at a center frequency of 1.98 GHz was designed with coupling elements,  $M_{S1} = M_{SL} = 1.1333$ ,  $M_{I2} = M_{34} = 0.97389$ ,  $M_{23} = 0.85305$ , and  $M_{14} = -0.24725$ .

Fig. 3.5-1 shows the ideal PII response for each stage of the 4-2 filter. The first four plots in Fig. 3.5-1 show the PII response for each stage without including the cross-coupling  $M_{14}$  and will be used as the references to tune the sequential main path couplings. The last plot in Fig. 3.5-1 shows

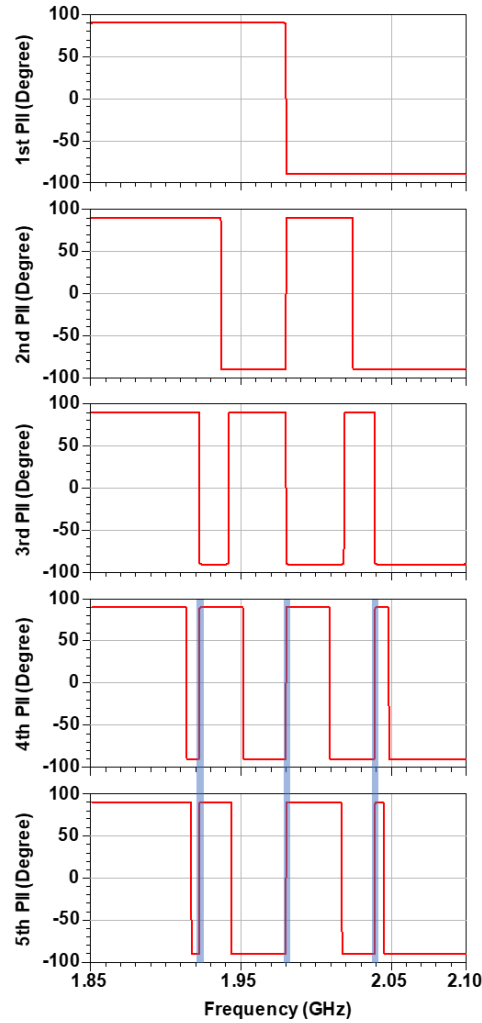


Fig. 3.5 - 1. Ideal PII responses of the elliptic filter at each design stage.



the PII response with all the main path couplings and the cross-coupling  $M_{14}$ . By comparing the last two plots in Fig. 3.5-1, one can see that the total number of phase transitions does not change, and that adding  $M_{14}$  only causes the locations of some phase transitions to shift. It is also interesting to observe that adding the cross-coupling  $M_{14}$  only affects the locations of the phase transition from  $+90^\circ$  to  $-90^\circ$ , whereas the locations of the phase transitions from  $-90^\circ$  to  $+90^\circ$  do not change, as illustrated in Fig. 3.5-1 (shown in thick lines).

Fig. 3.5-2 to Fig. 3.5-4 show that the 4-2 filter is tuned by matching the PII responses. At each stage, the resonant frequency of the newly added resonator is tuned first to ensure that the middle phase transition occurs at the center frequency of the filter. The newly introduced inter-resonator coupling is then tuned to match the ideal PII response. As mentioned in the previous section, the input coupling can be tuned by using the conventional method. Since  $M_{12} = M_{34}$ , all the main path couplings are well-tuned after the 3<sup>rd</sup> stage. In Fig. 3.5-4, one can clearly see that locations of the phase transitions from  $-90^\circ$  to  $+90^\circ$  are not affected when  $M_{14}$  is offset from its correct value.

Fig. 3.5-5 shows the physical model of a 4-2 combline filter. In practice, the physical realization of the filter usually contains the non-ideal physical I/O port, which can introduce an unexpected unknown transmission line between the physical reference plane and the port of the corresponding

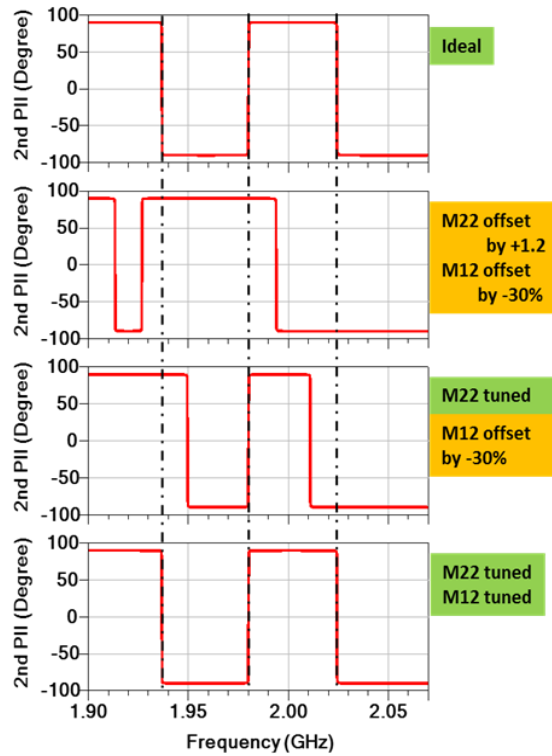


Fig. 3.5 - 2. The 2<sup>nd</sup> stage PII responses of the elliptic filter.

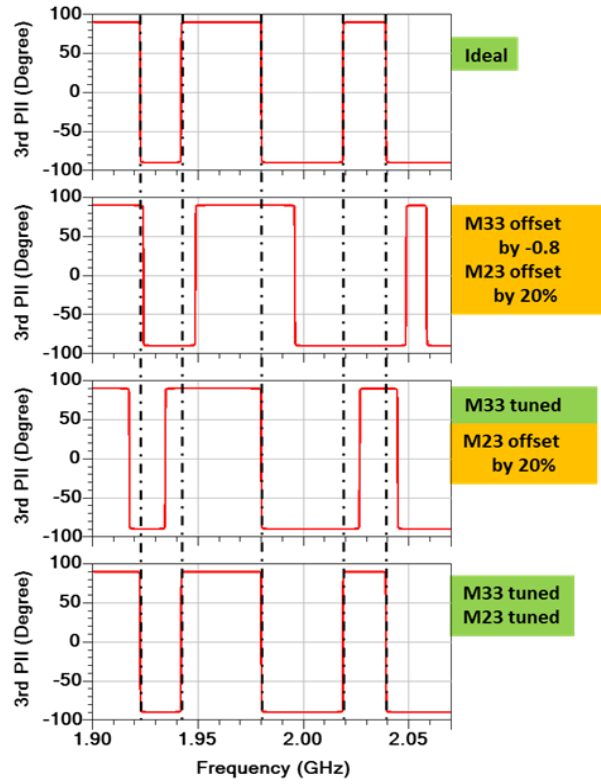


Fig. 3.5 - 3. The 3<sup>rd</sup> stage PII responses of the elliptic filter.

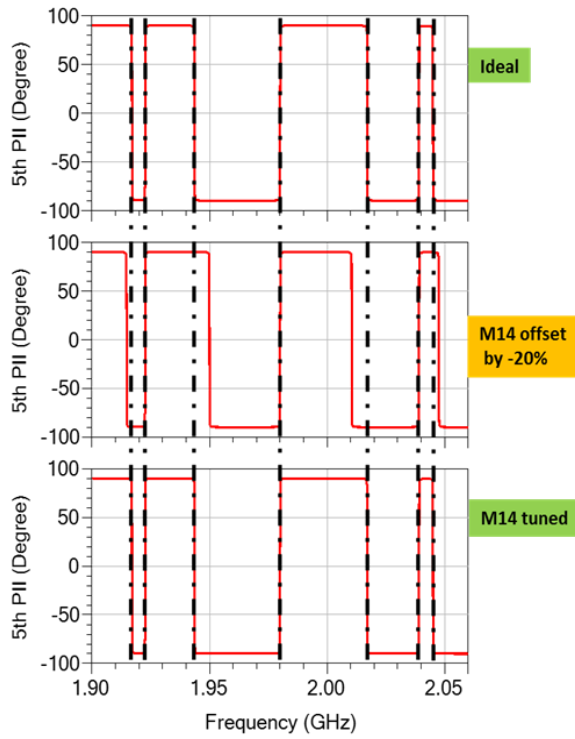


Fig. 3.5 - 4. The last stage PII responses of the elliptic filter.

inverter in the circuit model. Without taking into consideration the effects caused by the non-ideal physical I/O port, the accumulated errors during each design stage will become significant. Therefore, the first task in the filter-tuning process is to deal with the non-ideal I/O ports.

The non-ideal physical I/O ports mainly affect the phase of  $S_{11}$  and thus both the RGD (derivative of the phase of  $S_{11}$ ) response and the PII response will be affected at each design stage. The phase changes caused by the non-ideal physical input port will not affect the magnitude of  $S_{11}$ . Therefore, the input coupling and the 1<sup>st</sup> resonator's resonant frequency of the physical filter model can be well-tuned by matching the magnitude of  $S_{11}$  of the physical first resonator to that of the ideal circuit model. Once the input coupling and  $f_{R1}$  of the physical filter model are well-tuned, the non-ideal physical I/O port can be approximated by adding a transmission line with a specific electrical length in the circuit model, as shown in Fig. 3.5-6.

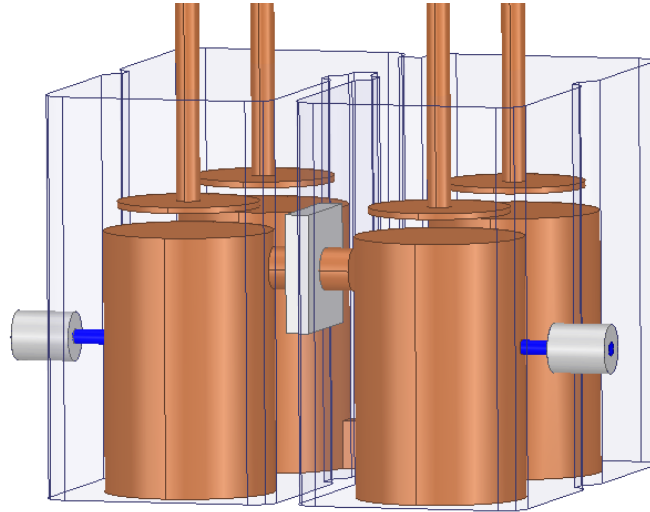


Fig. 3.5 - 5. The physical layout of the elliptic filter.

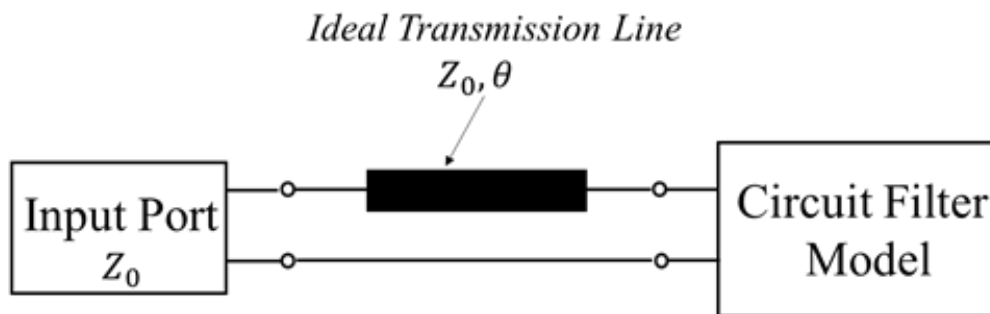


Fig. 3.5 - 6. Model the non-ideal input port as an ideal transmission line.

The steps can be summarized as follows:

- 1) Find the unloaded  $Q$  of the physical resonator.
- 2) Include  $Q$  in the circuit model.
- 3) Adjust  $M_{SI}$  and  $f_{RI}$  in the physical model until the magnitude of  $S_{II}$  matches that of the circuit model.
- 4) Add a transmission line in the circuit model, adjusting the electrical length of the added transmission line until its 1<sup>st</sup> stage PII response matches that of the physical model. The equivalent electrical length of the non-ideal physical I/O port is then extracted and added to the circuit model for the subsequent PII tuning stages. Alternatively, it can be used to de-embed the phase-loading from the physical model measurement.

The unloaded  $Q$  of the physical resonator can be easily determined experimentally or by using the eigenmode solution tool provided by ANSYS® HFSS. [9] Then, the identified unloaded  $Q$  is included in the circuit model. In the physical filter model, the tap position of the input probe and the height of the 1<sup>st</sup> resonator tuning screw are adjusted until the magnitude of  $S_{II}$  matches that of the circuit model.

Fig. 3.5-7 shows the 1<sup>st</sup> stage PII response of the physical model when  $M_{SI}$  and  $f_{RI}$  of the physical filter model are well-tuned. Rather than having one phase transition, the 1<sup>st</sup> stage PII response of the physical filter model has three phase transitions. The two extra phase transitions (in the blue shaded area) are caused by the additional input phase length of the actual physical unit.

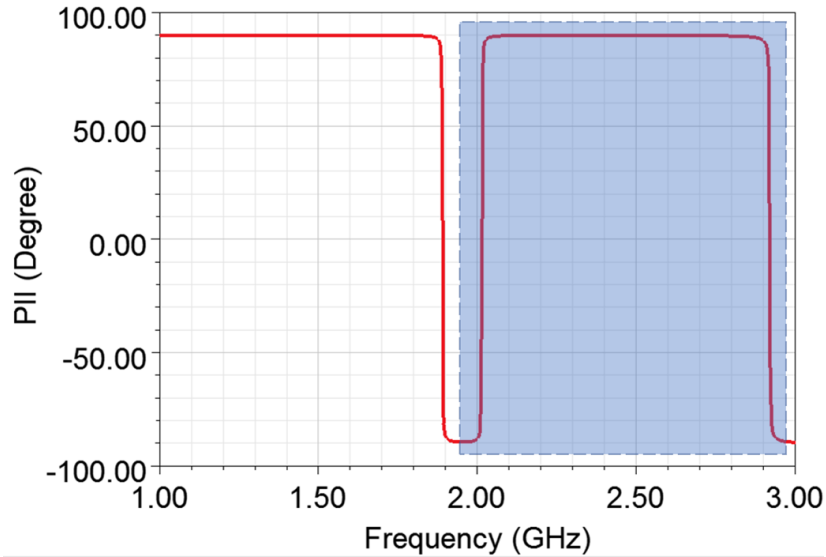


Fig. 3.5 - 7. The 1<sup>st</sup> stage PII response of the physical filter model after the input coupling is well-tuned.

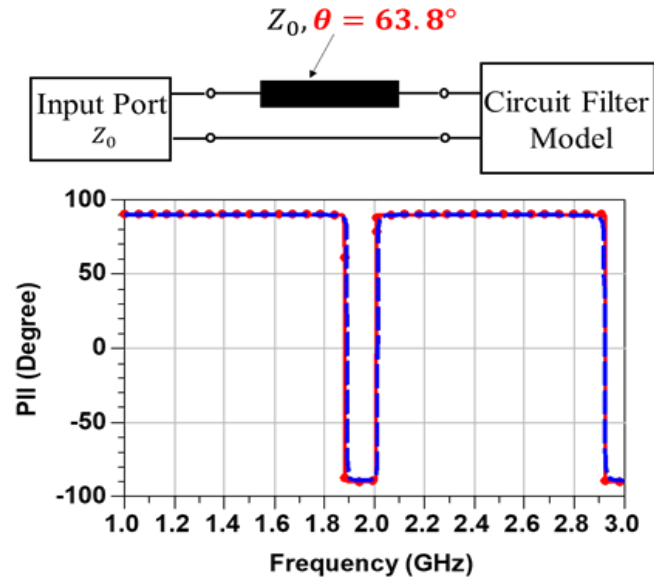


Fig. 3.5 - 8. Identifying the equivalent electrical length of the non-ideal input port.

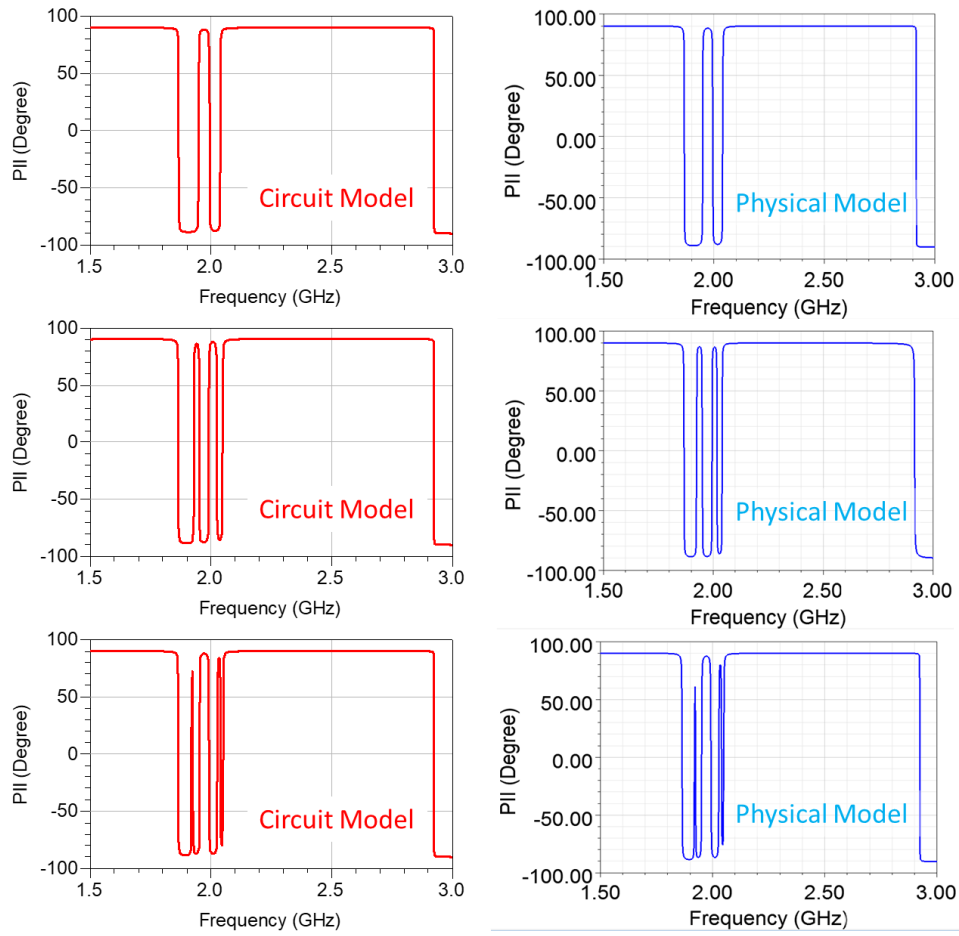


Fig. 3.5 - 9. PII responses of the new circuit model and the physical model for each design stage of the elliptic filter.

Next, an ideal transmission line is added to the circuit model and its electrical length is adjusted until its PII response matches the 1<sup>st</sup> stage PII response of the physical first combline resonator. Once the 1<sup>st</sup> stage PII responses of the circuit model and the physical model are matched, the equivalent electrical length of the physical input probe is determined, as shown in Fig. 3.5-8, which is found in this case to be 63.8°. The new circuit model is then used to generate reference PII responses for the following design stages.

Fig. 3.5-9 shows the PII responses of the new circuit model and the physical filter model. As one can see, the physical input probe generated two more phase transitions on the right-hand side of the passband for each design stage. The measured results of the tuned 4-2 combline filter are shown in Fig. 3.5-10.

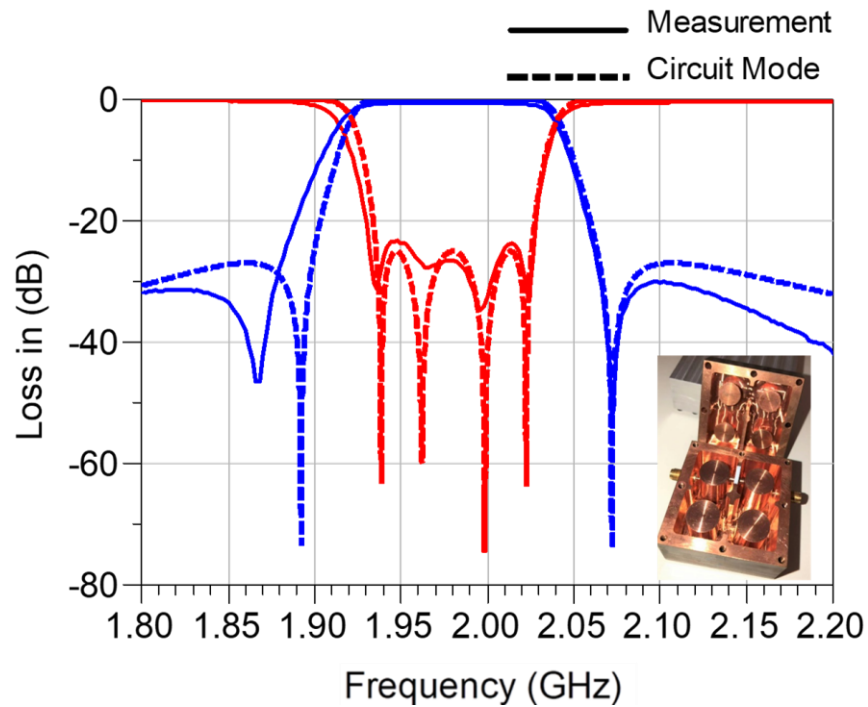


Fig. 3.5 - 10. The circuit simulation, the measurement results, and the photo of the elliptical filter.

### 3.6 Application of PII Technique to Diplexers

In this section, the proposed PII method is used to develop a diplexer sequentially. The diplexer consists of a T-junction and two CPW filters. Similar to the filter steps demonstrated in pervious sections, the development of the diplexer is segmented into several design stages, with a few elements needed to be adjusted at each stage. The CPW diplexer is designed by using a two-gold-layer structure built on a 635  $\mu\text{m}$  Alumina with a loss tangent of 0.0002 (shown in Fig. 3.6-1). The first gold layer is used to build the CPW circuit, while the second gold layer and the vias are used to realize crossovers for the CPW circuit.

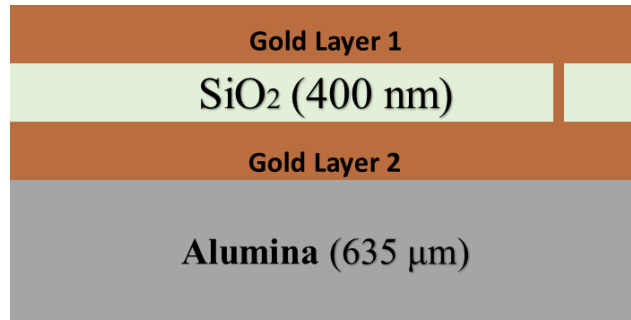


Fig. 3.6 - 1. Cross-section of two-gold-layer structure.

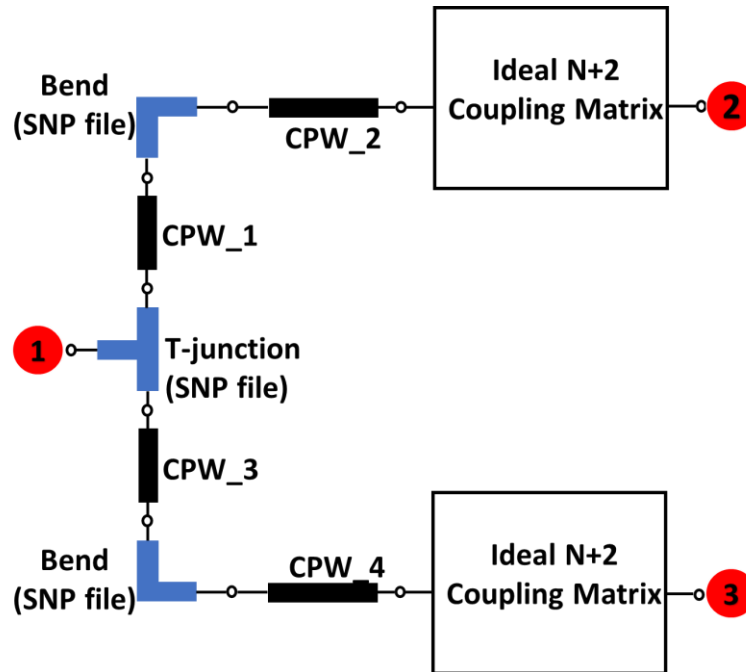


Fig. 3.6 - 2. Circuit model of the diplexer. Both coupling matrices have  $M_{S1} = M_{4L} = 1.0352$ ,  $M_{12} = M_{34} = 0.91058$ ,  $M_{23} = 0.69992$ , and zero the diagonal elements equal to zero.

The development of the diplexer using the PII method starts with constructing a circuit model [9]. As shown in Fig. 3.6-2, the circuit model contains a T-junction, two identical bands, CPW lines, and two ideal coupling matrices. Firstly, the T-junction (in Fig. 3.6-3) and the bend (in Fig. 3.6-4) are designed in SONNET®. The EM simulation results are then exported as SNP files and used in the circuit model.

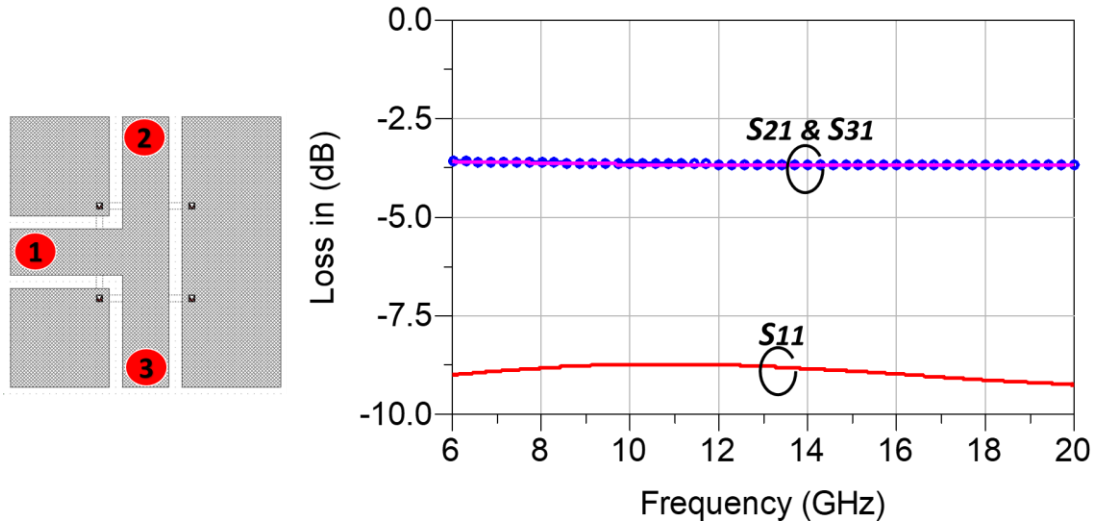


Fig. 3.6 - 3. Physical layout of the T-junction and its EM simulation results.

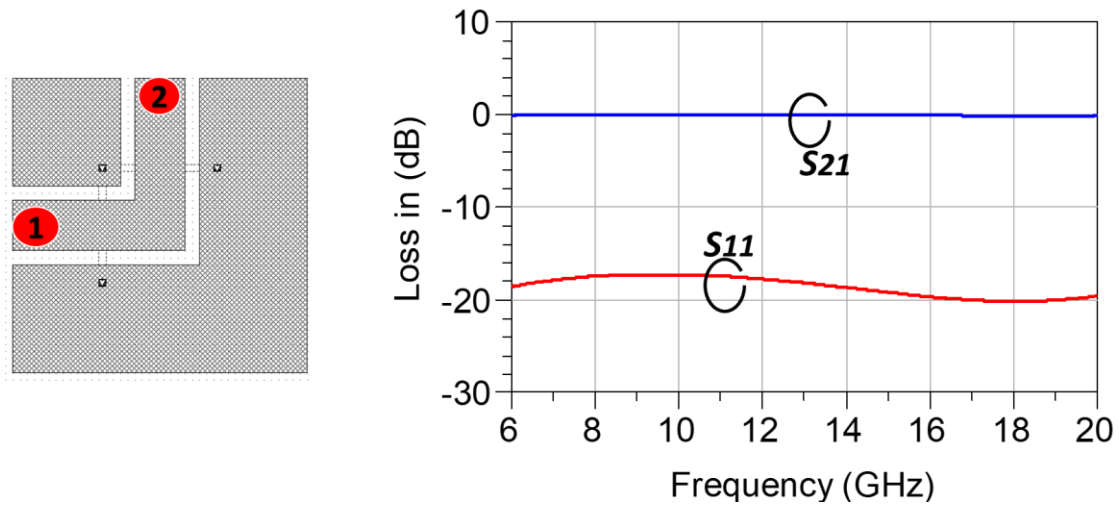


Fig. 3.6 - 4. Physical layout of the bend and its EM simulation results.



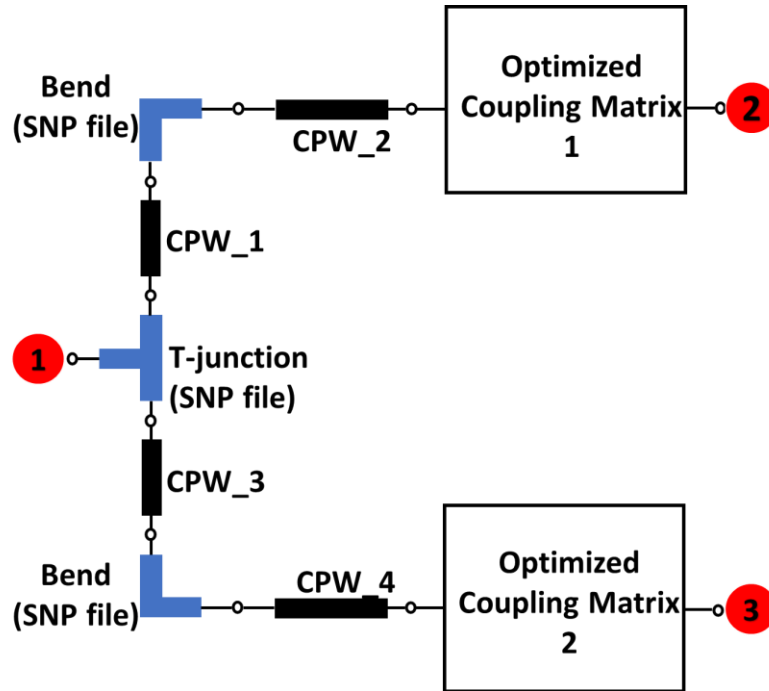


Fig. 3.6 - 5. Optimized circuit model of the diplexer. Coupling matrix 1:  $M_{S1} = 1.0356$ ,  $M_{12} = 0.94944$ ,  $M_{23} = 0.71466$ ,  $M_{34} = 0.91058$ ,  $M_{4L} = 1.0352$ ,  $M_{11} = 0.06825$ ,  $M_{22} = 0.10234$ ,  $M_{33} = 0.04747$ ,  $M_{44} = 0$ ; Coupling matrix 2:  $M_{S1} = 0.087832$ ,  $M_{12} = 0.89745$ ,  $M_{23} = 0.73618$ ,  $M_{34} = 0.91058$ ,  $M_{4L} = 1.0352$ ,  $M_{11} = 0.0297$ ,  $M_{22} = -0.06897$ ,  $M_{33} = -0.00389$ ,  $M_{44} = 0$ ; and zero the diagonal elements equal to zero.

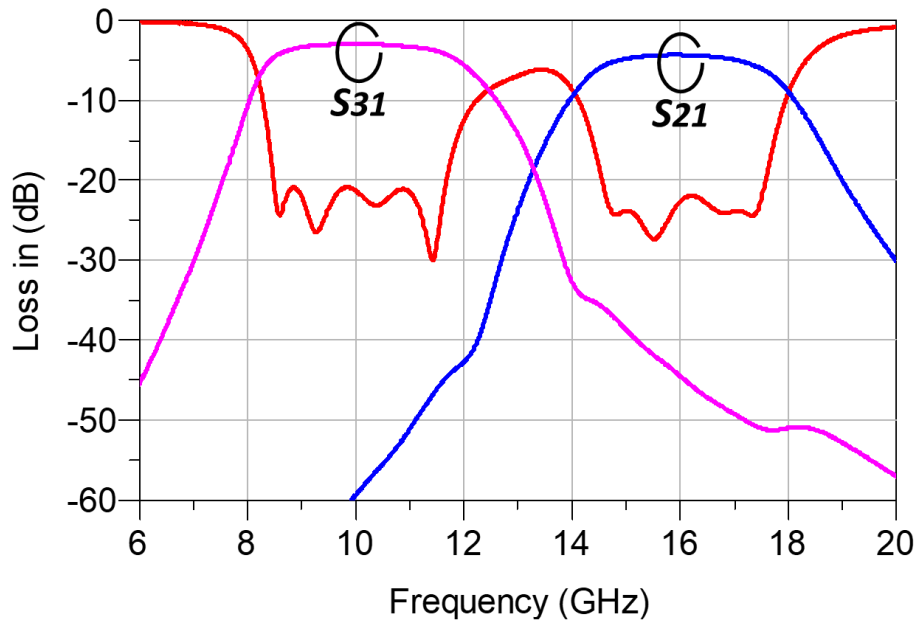


Fig. 3.6 - 6. Optimized circuit model simulation results.

Next, the length of the four CPW lines and the values of the coupling matrices in the circuit model are optimized (Fig. 3.6-5) to have the desired response (Fig. 3.6-6), using Keysight® ADS. This optimized circuit model is then used as the reference model, and the reference PII response of each design stage can be obtained.

The input couplings of the first two resonators of the two filters are first mapped into the physical dimensions by matching the reflected group delay, as shown in Fig. 3.6-7. The first resonators of the two filters are then connected with the common junction, as shown in Fig. 3.6-8, and the physical dimensions in the EM simulation are tuned to match the 1<sup>st</sup> stage reference model (i.e., the optimized circuit model in Fig. 3.6-5) PII response. Next, the successive resonators are added into the design circuits. Fig. 3.6-9 and Fig. 3.6-10 show that the design circuits are tuned to match the reference model PII responses for the 2<sup>nd</sup> and 3<sup>rd</sup> stages.

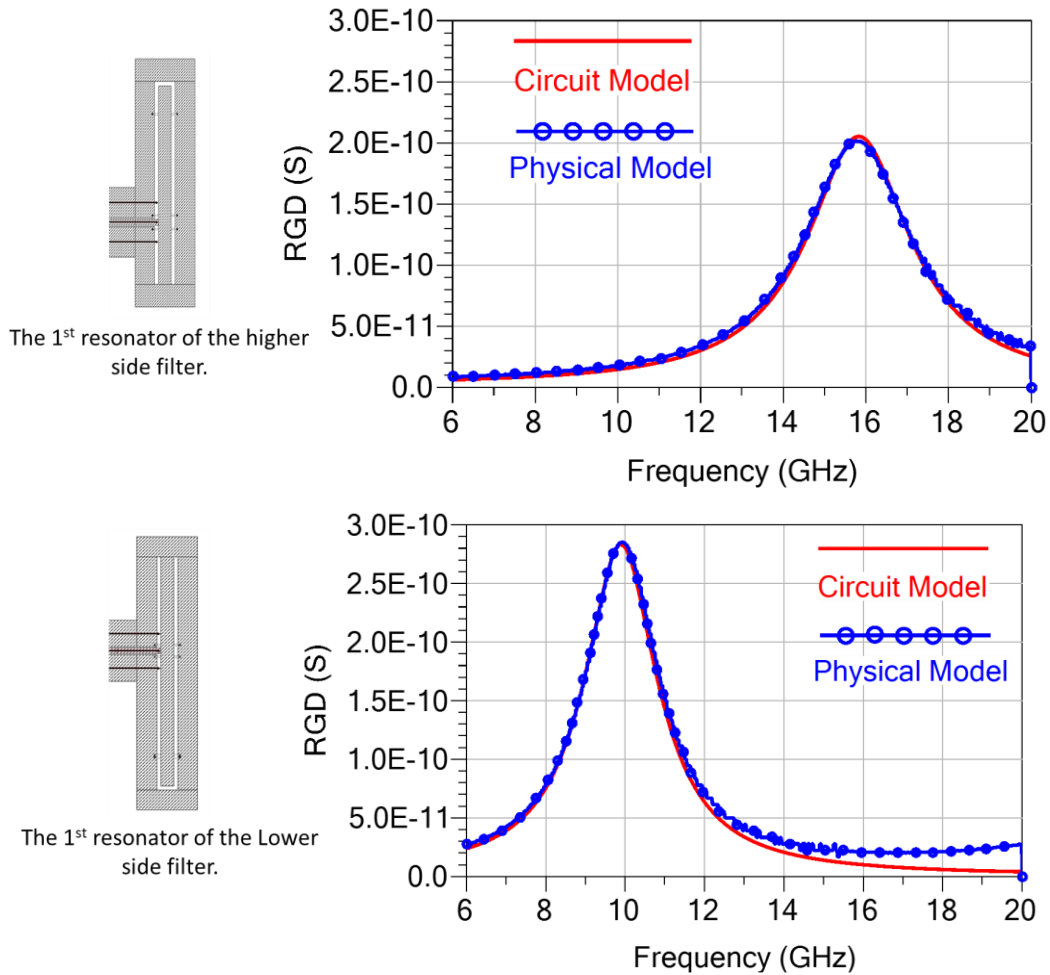


Fig. 3.6 - 7. Mapping input couplings of two filters into physical dimensions.

The output couplings of the last two resonators are mapped into the physical dimensions by matching the reflected group delay, as shown in Fig. 3.6-11. Finally, the 4<sup>th</sup> resonators of the two filters are joined with the 3<sup>rd</sup> stage design circuit, as shown in Fig. 3.6-12. Finally, the couplings  $M_{34}$  for both filters are mapped into the physical dimensions and final optimization is applied. The final EM simulation results of the designed diplexer are provided in Fig. 3.6-13.

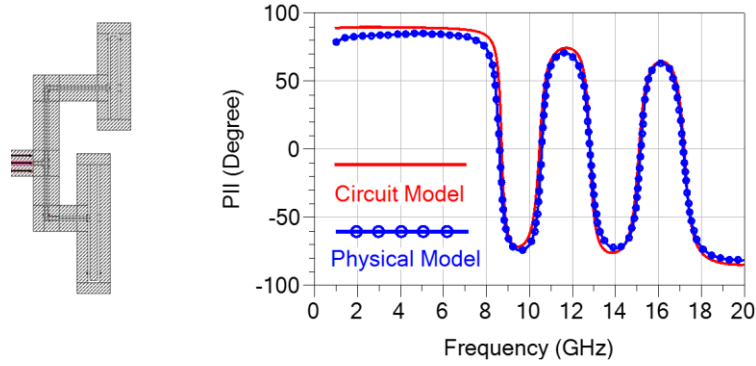


Fig. 3.6 - 8. The 1<sup>st</sup> stage PII response of the diplexer.

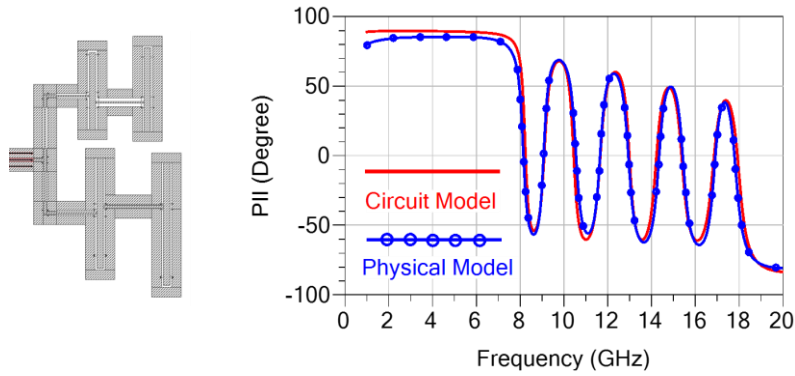


Fig. 3.6 - 9. The 2<sup>nd</sup> stage PII response of the diplexer.

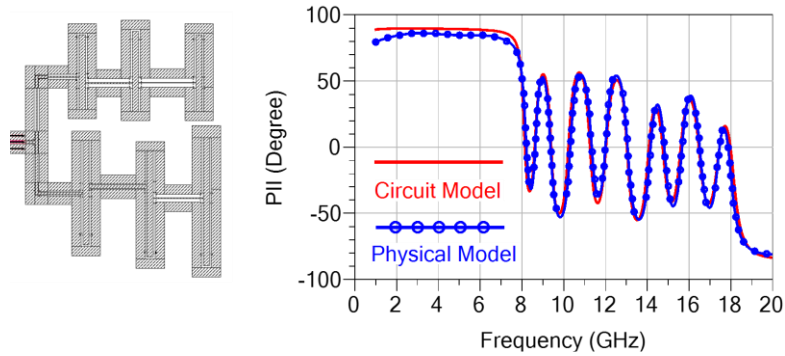


Fig. 3.6 - 10. The 3<sup>rd</sup> stage PII response of the diplexer.

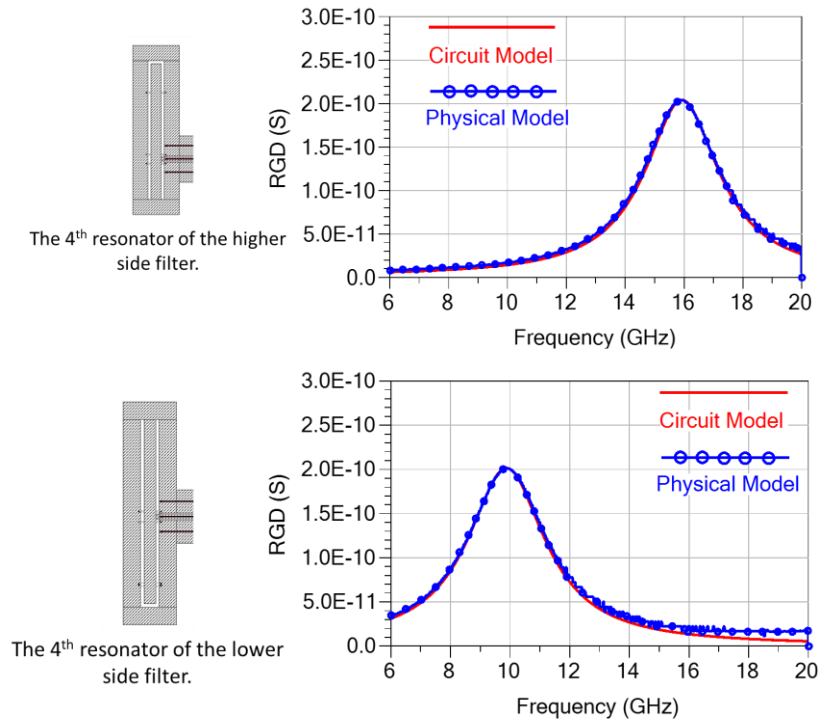


Fig. 3.6 - 11. Mapping the output couplings of the two filters into the physical dimensions.

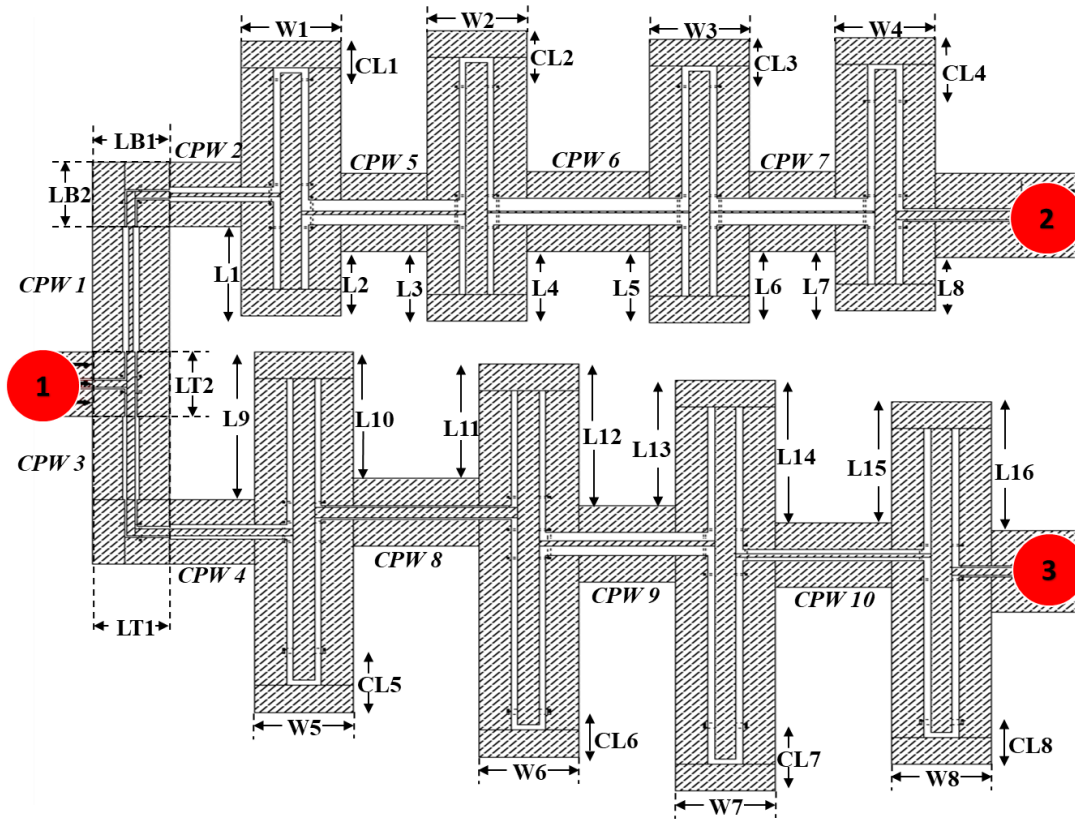


Fig. 3.6 - 12. The physical layout of the diplexer after adding the 4<sup>th</sup> resonators.

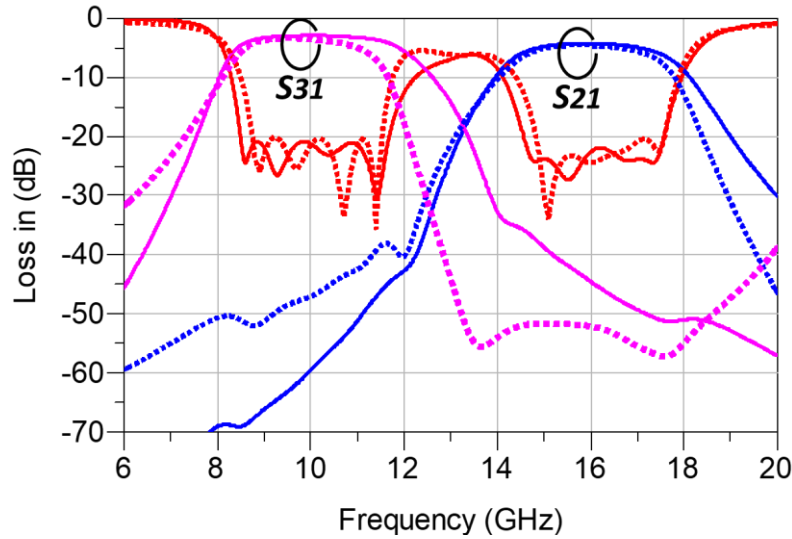


Fig. 3.6 - 13. Circuit model (solid lines) and EM simulation results (dashed lines).

### 3.7 Effect of Finite $Q$

As discussed in Section 3.2, the ideal PII response has a perfect square shape with only two states ( $\pm 90^\circ$ ) and phase transitions between them for the lossless case. Fig. 3.7-1 shows the 3<sup>rd</sup> stage PII circuit model response of a 4-pole Chebyshev bandpass filter, calculated using  $Q$  values of 100000, 2000, 200 and 20. As can be seen, the transitions of the PII response are still well-defined, even when dealing with  $Q$  values as low as 200. However, the transitions become less defined when dealing with very low  $Q$  values (20). Furthermore, the derivative of the PII response is maximum

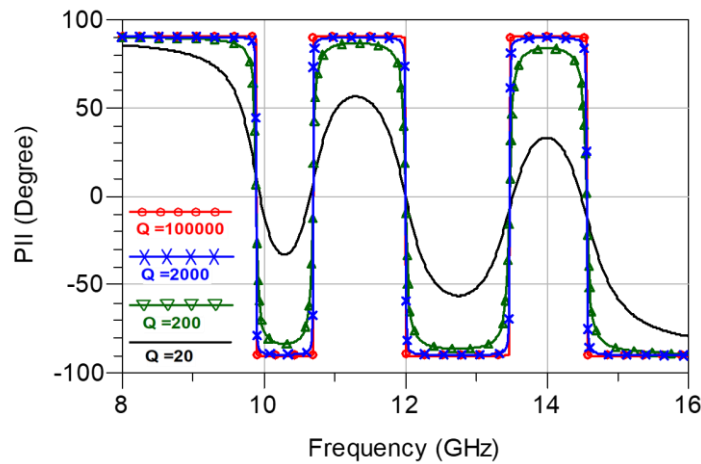


Fig. 3.7 - 1. The 3<sup>rd</sup> stage PII response of a 4-pole Chebyshev filter with different  $Q$  values.

at the phase transitions. In the case of very low  $Q$  values, one can use the derivative of the phase of the input impedance as a guide to identifying the locations of the transition points, as shown in Fig. 3.7-2. Thus, matching the derivative of the phase of the input impedance provides an alternative approach when dealing with the EM design of very low  $Q$  filters.

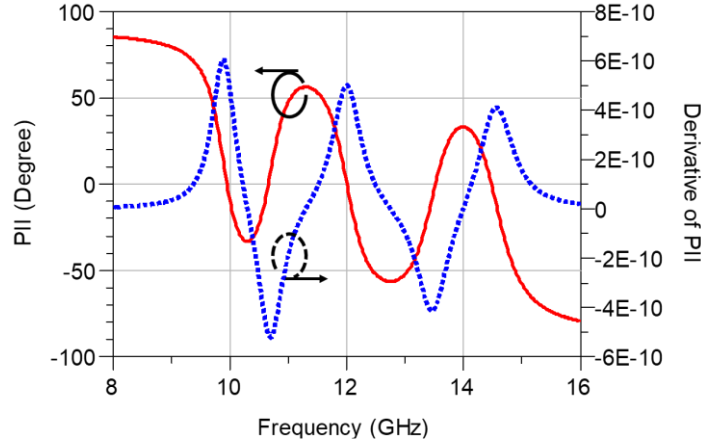


Fig. 3.7 - 2. The partial derivatives of the 3<sup>rd</sup> stage PII for the very low  $Q$  filter ( $Q=20$ ).

### 3.8 Discussion and Conclusion

The sequential tuning techniques, [31], [33], [41] and the new proposed PII technique presented in this paper apply the concept of “Divide and Conquer”, which results in an efficient approach in terms of increasing the design efficiency. The technique can be used in both filter EM-based designs and in tuning. The filter design/tuning process is divided into multiple stages. Thus, each incremental design stage requires less computation and optimization time. Instead of optimizing the entire filter parameters in one step. Only two parameters are optimized at each stage. At stage  $n$ , the two parameters are first initially optimized, then in order to take loading effects into consideration, the four parameters (the two parameters of stage  $n$  and the two parameters of the previous stage  $n-1$ ) may need to be fine optimized.

As shown in the examples given in this chapter, and those shown in [31], [33], [34], [35], and [41], the sequential technique provides reasonably good designs. It should be noted however, that application of this technique is not expected to lead to a design that can meet very tight specification requirements, for example, a requirement to have an exact equal ripple return loss over the filter bandwidth. Very fine tuning of the filter parameters may be needed to meet such tight requirements [27] - [29]. While, the proposed sequential technique works well for synchronously tuned filters

with or without cross-couplings, for narrowband asynchronously tuned filters with cross-couplings, the proposed sequential technique may not work well, since some of the phase transitions may overlap with each other.

This chapter introduced a new sequential filter design and tuning method that uses the phase of the input impedance as the design parameter. The novel approach was shown to require much less computation time than previous methods, since the distinguished information about the offsets in resonant frequencies and inter-resonator couplings can be acquired easily from the phase response of the input impedance. Closed-form expressions for the phase transition locations were provided. The method was then applied in designing an ultra-wideband filter, a narrowband 4-2 quasi-elliptic filter, and a wideband diplexer. Furthermore, the PII response was used to extract the equivalent electrical length of the unknown transmission line caused by the non-ideal filter physical I/O ports. Finally, the effect of finite  $Q$  was discussed, and an alternative design parameter response proposed for dealing with the design and tuning of very low  $Q$  filters.

Table 3.1. The 1 <sup>st</sup> Four Stage Phase Transition Locations in Terms of Coupling Matrix Element Values				
Phase Transition	Stage 1	Stage 2	Stage 3	Stage 4
$\omega_6$				$\frac{\sqrt{2}}{4(\Delta\omega_0)^{-1}} \left( \sqrt{M_{12}^2 + M_{23}^2 + M_{34}^2 + 8\frac{1}{\Delta^2} + S} - \sqrt{M_{12}^2 + M_{23}^2 + M_{34}^2 + S} \right)$
$\omega_4$			$\frac{\sqrt{M_{12}^2 + M_{23}^2 + 4\frac{1}{\Delta^2}} - \sqrt{M_{12}^2 + M_{23}^2}}{2(\Delta\omega_0)^{-1}}$	$\frac{\sqrt{M_{23}^2 + M_{34}^2 + 4\frac{1}{\Delta^2}} - \sqrt{M_{23}^2 + M_{34}^2}}{2(\Delta\omega_0)^{-1}}$
$\omega_2$		$\frac{\sqrt{M_{12}^2 + 4\frac{1}{\Delta^2}} - M_1}{2(\Delta\omega_0)^{-1}}$	$\frac{\sqrt{M_{23}^2 + 4\frac{1}{\Delta^2}} - M_{23}}{2(\Delta\omega_0)^{-1}}$	$\frac{\sqrt{2}}{4(\Delta\omega_0)^{-1}} \left( \sqrt{M_{12}^2 + M_{23}^2 + M_{34}^2 + 8\frac{1}{\Delta^2} - S} - \sqrt{M_{12}^2 + M_{23}^2 + M_{34}^2 - S} \right)$
$\omega_1$	$\omega_0$	$\omega_0$	$\omega_0$	$\omega_0$
$\omega_3$		$\frac{\sqrt{M_{12}^2 + 4\frac{1}{\Delta^2}} + M_1}{2(\Delta\omega_0)^{-1}}$	$\frac{\sqrt{M_{23}^2 + 4\frac{1}{\Delta^2}} + M_{23}}{2(\Delta\omega_0)^{-1}}$	$\frac{\sqrt{2}}{4(\Delta\omega_0)^{-1}} \left( \sqrt{M_{12}^2 + M_{23}^2 + M_{34}^2 + 8\frac{1}{\Delta^2} - S} + \sqrt{M_{12}^2 + M_{23}^2 + M_{34}^2 - S} \right)$
$\omega_5$			$\frac{\sqrt{M_{12}^2 + M_{23}^2 + 4\frac{1}{\Delta^2}} + \sqrt{M_{12}^2 + M_{23}^2}}{2(\Delta\omega_0)^{-1}}$	$\frac{\sqrt{M_{23}^2 + M_{34}^2 + 4\frac{1}{\Delta^2}} + \sqrt{M_{23}^2 + M_{34}^2}}{2(\Delta\omega_0)^{-1}}$
$\omega_7$				$\frac{\sqrt{2}}{4(\Delta\omega_0)^{-1}} \left( \sqrt{M_{12}^2 + M_{23}^2 + M_{34}^2 + 8\frac{1}{\Delta^2} + S} + \sqrt{M_{12}^2 + M_{23}^2 + M_{34}^2 + S} \right)$
<p>where, <math>\Delta = \frac{BW}{\omega_0}</math></p> $S = \sqrt{M_{12}^4 + M_{23}^4 + M_{34}^4 + 2M_{12}^2 M_{23}^2 + 2M_{23}^2 M_{34}^2 - 2M_{12}^2 M_{34}^2}$				



Table 3.2 DIMENSIONS OF THE DIPLEXER IN FIG. 3.6-12 (Unit in $\mu\text{m}$ )							
Common Junction							
<i>T- Junction</i>							
Signal Line Width	4	Slot Width	10	LT1	360	LT2	360
<i>Bend</i>							
Signal Line Width	40	Slot Width	10	LB1	360	LB2	360
<i>CPW 1</i>							
Signal Line Width	20	Slot Width	30	Length	700		
<i>CPW 2</i>							
Signal Line Width	20	Slot Width	30	Length	480		
<i>CPW 3</i>							
Signal Line Width	40	Slot Width	20	Length	470		
<i>CPW 4</i>							
Signal Line Width	40	Slot Width	20	Length	540		
Higher Band Filter							
<i>Resonator 1</i>							
Signal Line Width	100	Slot Width	30	L1	500	L2	360
Signal Line Length	1210	CL1	210	W1	460		
<i>CPW 5</i>							
Signal Line Width	20	Slot Width	60	Length	700		
<i>Resonator 2</i>							
Signal Line Width	100	Slot Width	30	L3	390	L4	390
Signal Line Length	1300	CL2	310	W2	460		
<i>CPW 6</i>							
Signal Line Width	10	Slot Width	70	Length	870		
<i>Resonator 3</i>							
Signal Line Width	100	Slot Width	30	L5	400	L6	400
Signal Line Length	1260	CL3	260	W3	460		
<i>CPW 7</i>							
Signal Line Width	10	Slot Width	70	Length	700		
<i>Resonator 4</i>							
Signal Line Width	100	Slot Width	30	L7	330	L8	300
Signal Line Length	1200	CL4	350	W4	460		
<i>Output Port CPW</i>							
Signal Line Width	50	Slot Width	10				
All the crossovers have the width of 10 $\mu\text{m}$ .							
Lower Band Filter							
<i>Resonator 1</i>							
Signal Line Width	100	Slot Width	30	L9	830	L10	710
Signal Line Length	1690	CL5	330	W5	460		
<i>CPW 8</i>							
Signal Line Width	60	Slot Width	10	Length	880		
<i>Resonator 2</i>							
Signal Line Width	100	Slot Width	30	L11	640	L12	790
Signal Line Length	1870	CL6	240	W6	460		
<i>CPW 9</i>							
Signal Line Width	30	Slot Width	50	Length	750		
<i>Resonator 3</i>							
Signal Line Width	100	Slot Width	30	L13	700	L14	800
Signal Line Length	1970	CL7	350	W7	460		
<i>CPW 10</i>							
Signal Line Width	20	Slot Width	20	Length	840		
<i>Resonator 4</i>							
Signal Line Width	100	Slot Width	30	L15	680	L16	720
Signal Line Length	1700	CL8	220	W8	460		
<i>Output Port CPW</i>							
Signal Line Width	40	Slot Width	10				
All the crossovers near the open ends have the width of 30 $\mu\text{m}$ , and all other crossovers have the width of 10 $\mu\text{m}$ .							

# Chapter 4

## Niobium-Based mm-Wave Ultra-Wideband Filters and Multiplexers

### 4.1 Introduction

Superconductor Micro-Electronics technology (SME) allows for the realization of digital receivers capable of directly digitalizing frequency (RF) signals up to several hundred gigahertz with very low power consumption [47]-[48]. Figure 4.1-1 shows a simple block diagram of an SME digital RF receive consisting of an analogue front-end and superconductor analogue-to-digital converter (ADC). The ADCs are realized using rapid single-flux quantum (RSFQ) logic. While superconductor ADCs are capable of digitizing very wideband RF signals, the current technology of RSFQ logic makes it more feasible and efficient to implement superconductor ADC with a bandwidth of 20-30 GHz.

To deal with wider band signals, several ADCs and a wideband millimeter-wave (mm-Wave) channelizer can be used, as shown in Fig. 4.1-1. The ability to integrate a monolithic triplexer up to mm-Wave frequencies with ADCs on a single chip will enhance the RF performance of a digital receiver and reduce its overall size. To achieve a single chip solution for the receiver in Fig. 4.1-1, there are several challenges for developing the desired mm-Wave triplexer. First, ultra-wideband

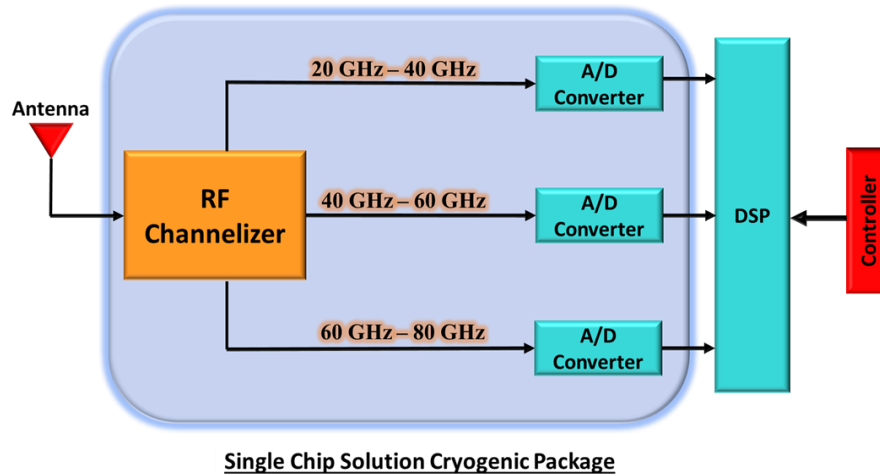


Fig. 4.1 - 1. The schematic of the SME digital receiver.

(UWB) superconductor filters with a fractional bandwidth greater than 60% are required. Secondly, the manifold used to connect all the filters must be able to operate over a broad frequency band. Also, the harmonics of the lowest frequency channel filter need to be treated more strictly, as its harmonics can interfere with the other filters in the triplexer. At the same time, however, cross-couplings due to radiation between planar filters integrated on one substrate complicate the design. Furthermore, the physical size of the triplexer should be highly miniaturized so that it can be monolithically integrated with the ADCs in a single chip cryogenic package.

This chapter focuses on realizing a triplexer with all the aforementioned challenges conquered. First, a multi-layer Nb-based superconductor bandpass filter operating over the frequency range 30 GHz - 60 GHz is demonstrated in section 4.2. The filter is realized in a co-planar waveguide (CPW) structure, where crossovers in the multilayer structure are employed to reduce the filter size. The section also illustrates how these crossovers can be utilized to fine-tune the filter performance. An 8-pole superconductor niobium-based filter with a size of 0.88 mm x 2.2 mm and designed with a center frequency of 45 GHz and a bandwidth of 30 GHz is developed, fabricated, and tested. Next, an Nb-based wideband superconductor mm-Wave noncontiguous diplexer is demonstrated in section 4.3. This diplexer has two channels, namely 25 GHz - 35GHz and 40 GHz - 50 GHz. Finally, section 4.4 demonstrates the feasibility of realizing an Nb-based mm-Wave UWB superconductor contiguous triplexer. The triplexer covers the frequency range from 20 GHz to 80 GHz, offering three contiguous channels of 20 GHz bandwidth each.

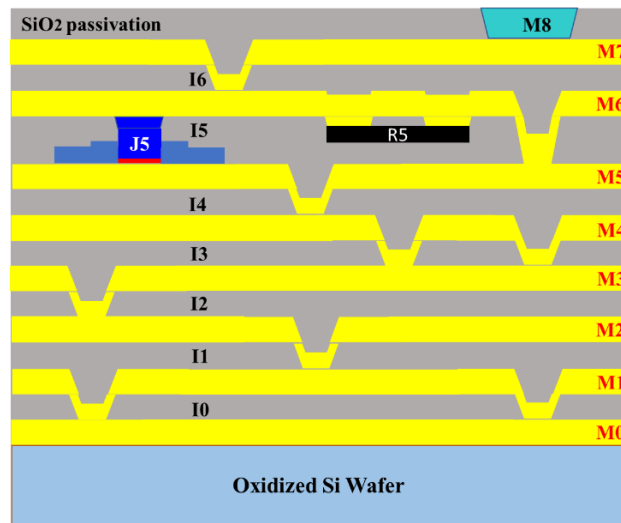


Fig. 4.1 - 2. The cross section of the MIT-LL 8-niobium-layer fabrication process. [50]

The designed filter and multiplexers are fabricated using the MIT Lincoln Laboratory (MIT-LL) 8-niobium (Nb)-layer fabrication process shown in Fig. 4.1-2 [49]. In this process, there are 8 niobium layers (M0 - M7) and silicon dioxide ( $\text{SiO}_2$ ) layers in between. Each Nb layer has a thickness of 200 nm, and all the Nb layers can be connected using vias (I0 - I6). The height of each via is 200 nm, except Via I5 has a height of 280 nm. Moreover, Layer J5 is used to realize Josephson junctions, and the lossy conductor layer, R5, with a thickness of 40 nm, can be used to realize resistive terminals. The gold layer, M8, with a thickness of 250 nm, can be used for landing pads.

## 4.2 Nb-Based mm-Wave UWB Superconductor Filter

The MIT-LL 8-Nb-layer process allows for the realization of different types of planar transmission line structures, such as microstrip lines, coplanar waveguides (CPW), and strip lines. CPW lines offer better RF performance (i.e., less radiation and dispersion effects) than microstrip lines at mm-Wave frequencies and have more design flexibility than the strip lines. Therefore, CPW resonators are selected to develop the proposed mm-Wave UWB bandpass filter. In this design, the CPW signal lines are realized on the first Nb layer (M7), which is shown in green in the schematic given in Fig. 4.2-1. Ground planes of the CPW lines are realized on all the Nb layers and connected using vias, which are shown in red in Fig. 4.2-1. Metal ground planes are inserted in the 8 Nb layers in order to satisfy the metal fill requirements of the MIT-LL 8-Nb-layer process.

In comparison to the strip line and microstrip line resonators, CPW resonators exhibit a larger circuit size due to their lower effective dielectric constant. Moreover, crossovers are required by the CPW line for suppressing unexpected propagation modes. Such crossovers can significantly

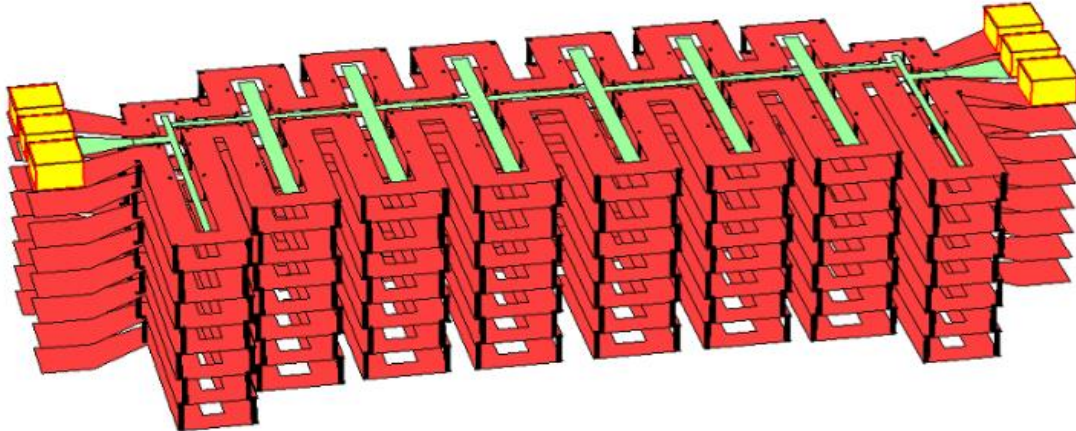


Fig. 4.2 - 1. The 3D layout of the multi-layer millimeter-wave UWB bandpass filter. Only the 1<sup>st</sup> Nb layer is used as the functional signal layer; the subsequent 7 Nb layers are used for additional ground planes and optional crossovers.

affect both the physical size and RF performance at mm-Wave frequencies of CPW resonators. By adding crossovers into the CPW circuit, capacitances with relatively high values between the CPW signal lines and ground are introduced (e.g.,  $C_1$  and  $C_2$  in Fig. 4.2-2). When crossovers have a small height or a large width, the extra capacitance becomes significantly large, loading the transmission lines and changing the resonance frequency of the resonators. Traditionally, the locations of crossovers in CPW circuits are selected strategically far away from areas where the E-field is high in order to reduce the impact of their loading. In this chapter the crossovers are used to intentionally generate extra capacitances in the design to help miniaturize the filter size and fine-tune its performance.

Most EM-based filter design techniques effectively deal with the design of relatively narrowband filters ( $BW < 10\%$ ) [9]. The EM-based design complexity of developing a mm-Wave UWB bandpass filters can be reduced by using the recently developed PII method introduced in Chapter 3.

In the MIT-LL 8-Nb-layer process, the silicon dioxide layers have a thickness of around 200 nm and the thickness of the niobium layers is also around 200 nm. Thus, crossovers with different heights can be realized by placing them on different niobium layers. Figure 4.2-3 shows a single resonator with the tapped input. This CPW signal line is built on the first niobium layer, and ground strips are built on all the Nb layers connected with vias. Figure 4.2-3 (a) also shows the EM simulation results for the resonator, with crossovers having the same width of 5  $\mu\text{m}$  built on the 2<sup>nd</sup>

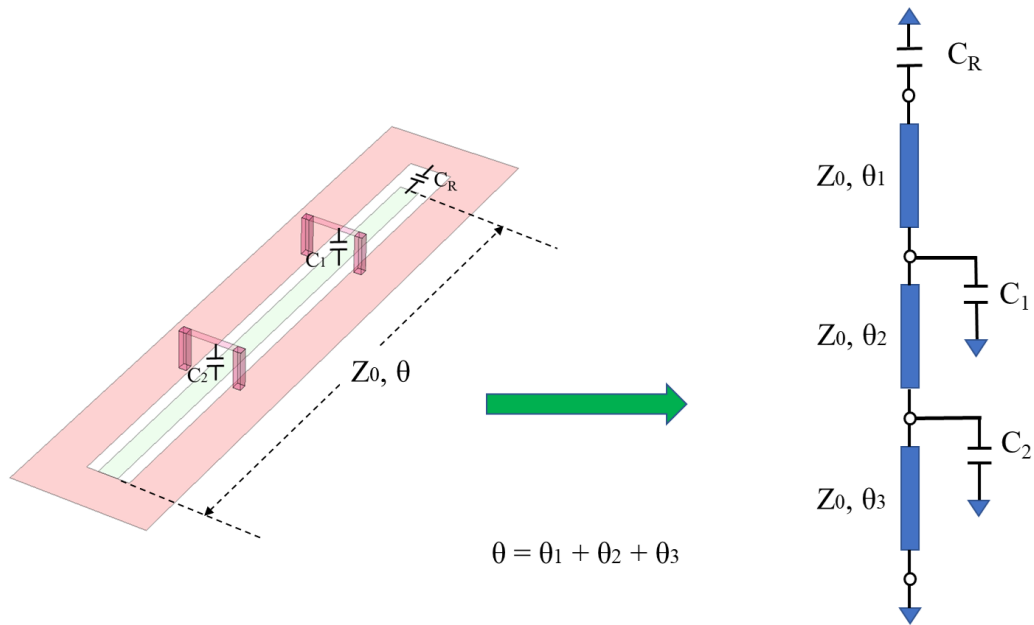
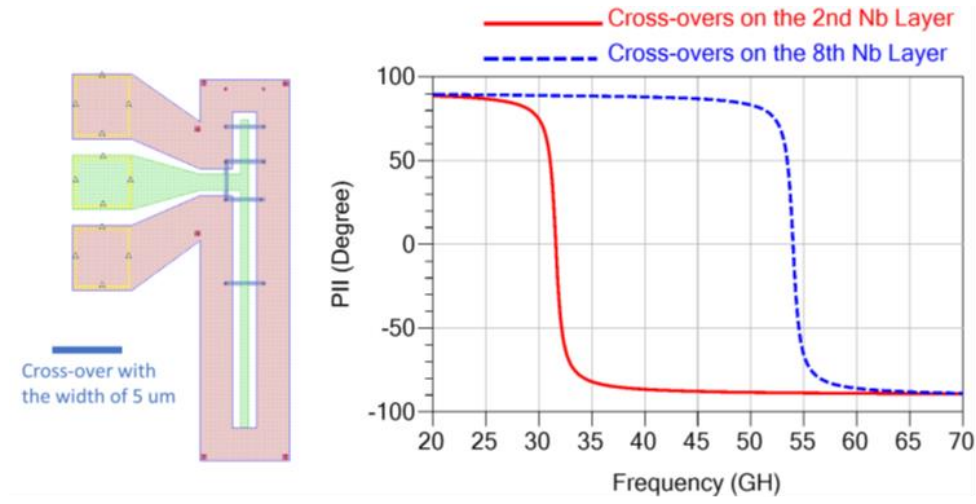
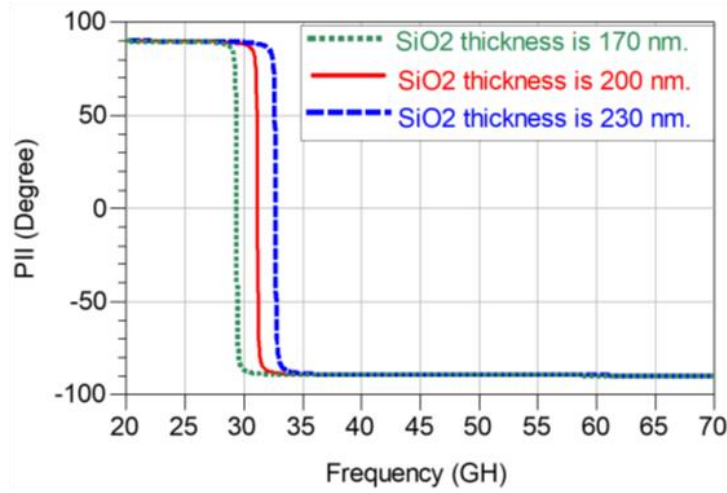


Fig. 4.2 - 2. The CPW resonator with crossovers and its equivalent circuit.



(a)



(b)

Fig. 4.2 - 3.(a) EM simulation results for crossovers realized on different Nb layers. (b) EM simulation results for SiO<sub>2</sub> layers with different thickness.

(plot in red) and 8<sup>th</sup> (plot in blue) Nb layers, respectively. When the crossovers are on the 2<sup>nd</sup> Nb layer, the height is 200 nm; and when the crossovers are on the 8<sup>th</sup> Nb layer, the height is around 2.6  $\mu\text{m}$ . As explained in Chapter 3, for a single ideal parallel LC resonator, the phase of the input impedance has only two states (i.e.,  $\pm 90^\circ$ ), and a phase transition from  $+90^\circ$  to  $-90^\circ$  emerges at the resonant frequency. As can be seen in Fig. 4.2-3 (a), when the height of the crossovers is reduced from 2.6  $\mu\text{m}$  to 200 nm, the capacitance introduced by the crossovers increases significantly, leading to a shift in the resonant frequency from 54 GHz to 31 GHz. As a consequence of realizing

the crossovers with such a small height, the physical size of the millimeter-wave CPW resonator is reduced by 57%. Moreover, the process tolerance for the thickness of the SiO<sub>2</sub> layer is  $\pm 30$   $\mu\text{m}$ . Figure 4.2-3 (b) presents the EM simulation results for a resonator with crossovers having the same width of 5  $\mu\text{m}$  built on the 2<sup>nd</sup> Nb layer, for the three thickness values of 170 nm, 200 nm, and 230 nm for the SiO<sub>2</sub> layer between the 1<sup>st</sup> and 2<sup>nd</sup> Nb layers. As shown, the resonant frequency of the CPW resonator in this example can have a  $\pm 5\%$  shift due to the fabrication process tolerances.

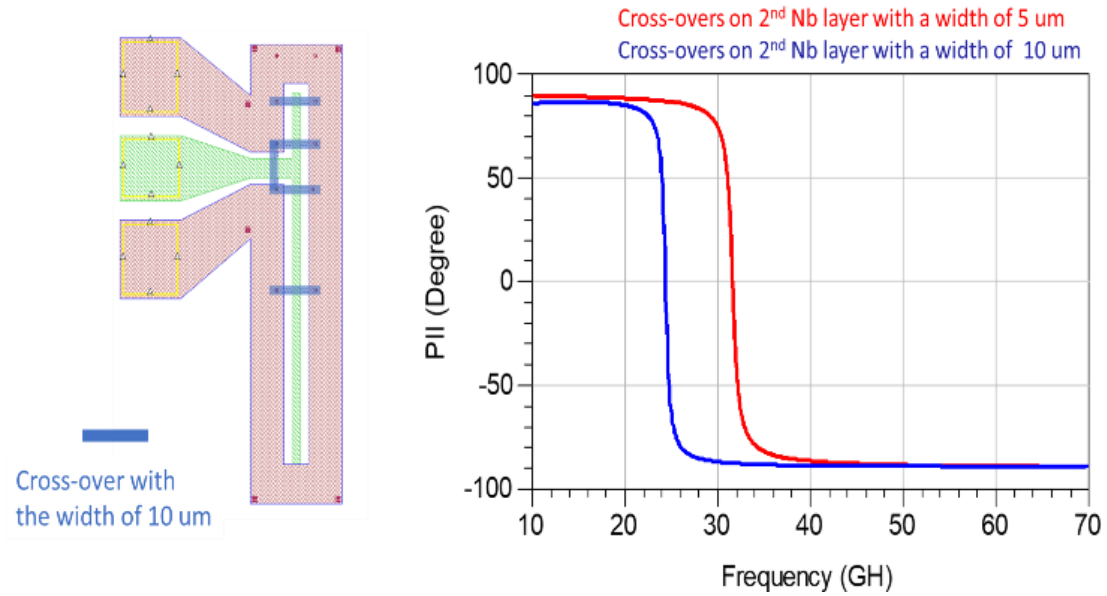


Fig. 4.2 - 4. EM simulation results for crossovers on the 2nd Nb layer with different widths.

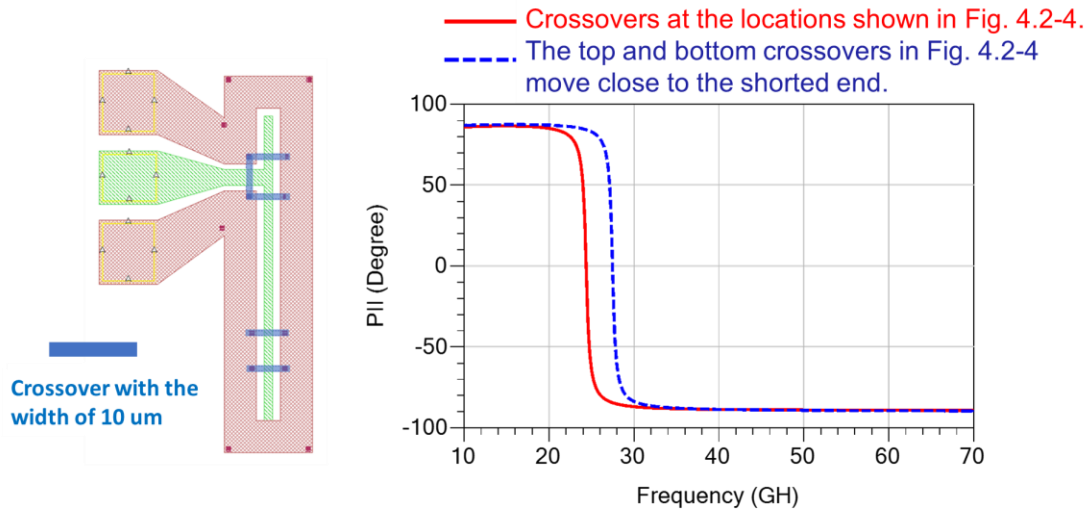


Fig. 4.2 - 5. EM simulation results for the crossovers located at different places.



By using the MIT-LL 8-Nb-layer process, the lowest height of the crossover is 200 nm. To further increase capacitance loading, the width of the crossovers can be increased. Figure 4.2-4 illustrates a scenario where all the crossovers are built on the 2<sup>nd</sup> Nb layer. As the width of the crossovers increases from 5  $\mu\text{m}$  to 10  $\mu\text{m}$ , the resonant frequency shifts from 31 GHz to 24 GHz. Similarly, the resonant frequency increases if the width of the crossovers decreases.

As mentioned above, the location of the crossover is also important for controlling the loading effects. This gives the designer another degree of freedom to control the capacitance loading and hence the resonance frequency of the resonator. In Fig. 4.2-5, both the top and bottom crossovers are relocated from their positions shown in Fig. 4.2-4, with the resonant frequency shifting upward by around 10%.

The above three examples demonstrate that the extra capacitances introduced through the use of crossovers can help to miniaturize the design. Similarly, they can be used for fine-tuning the resonance frequencies of the resonators. Furthermore, fine-tuning the inter-resonator coupling can be accomplished by adjusting the locations and widths of the crossovers. Figure 4.2-6 shows two CPW resonators coupled by a CPW bridge between the resonators. Normally, in order to fine-tune the coupling between the resonators, either the length of the CPW bridge or the tapping positions at the two resonators need to be varied. Alternatively, the coupling can be tuned by varying the capacitive loading through the selection of height, size and location of the crossovers mounted over the CPW bridge. As shown in Fig. 4.2-6, by simply increasing the width of the two crossovers in the dashed circuits, all three phase transition locations shift to lower frequencies with the same amount of 2 GHz. Based on the tuning method introduced in Chapter 3, the change in frequency

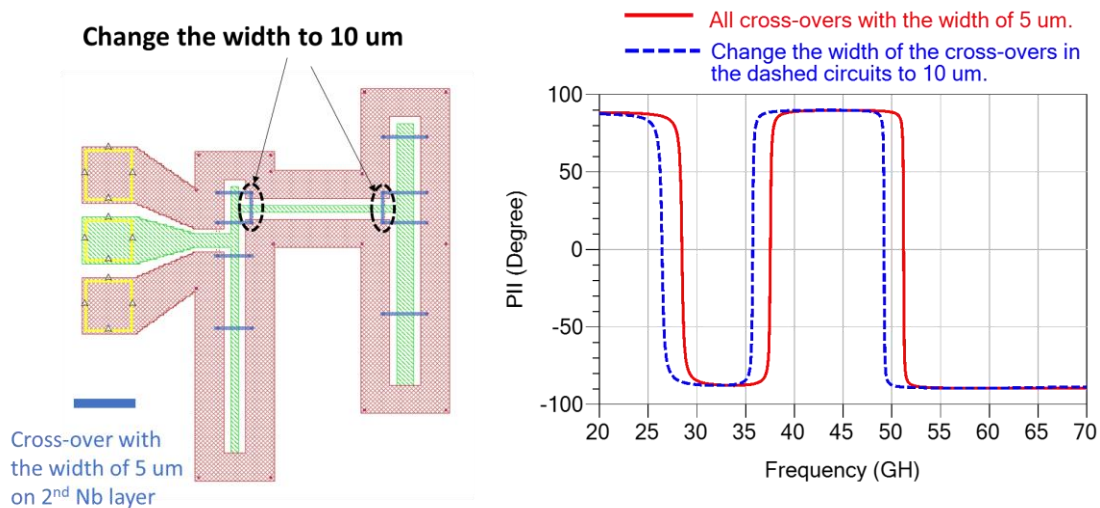


Fig. 4.2 - 6. EM simulation results for the design circuits with two coupled resonators.



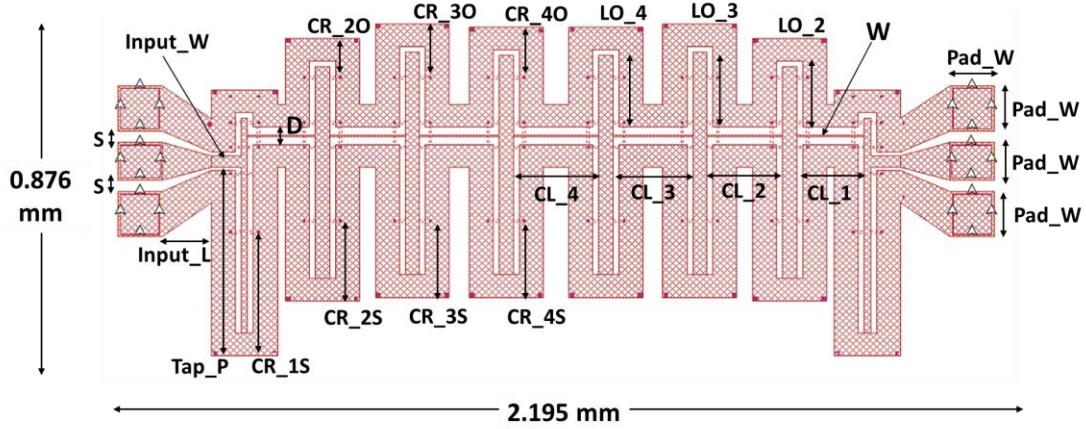


Fig. 4.2 - 7. The 2D layout of the designed mm-Wave superconductor UWB bandpass CPW filter.

locations of the transitions is attributed to a change in the inter-resonator coupling value.

Figure 4.2-7 depicts the top 2D layout view of the mm-Wave superconductor UWB bandpass CPW filter with landing pads for measurement. This 8-pole filter is physically symmetric. The signal lines of the CPW are realized on the 1<sup>st</sup> Nb layer, and ground planes of the CPW lines are realized on all Nb layers connected using vias. The filter dimensions are 2.195 mm x 0.876 mm (including the landing pads). The width of the signal lines of the 1<sup>st</sup> and 8<sup>th</sup> CPW resonator is 15  $\mu\text{m}$ , and all the other CPW resonators have signal lines with a width of 35  $\mu\text{m}$ . The gap for all the CPW resonators is 15  $\mu\text{m}$ . Further, all the crossovers are realized on the 2<sup>nd</sup> Nb layer and have a

Table 4.1			
PHYSICAL DIMENSIONS OF THE FILTER IN FIG.4.2-7			
Symbol	Value ( $\mu\text{m}$ )	Symbol	Value ( $\mu\text{m}$ )
<i>Input_W</i>	30	<i>W</i>	5
<i>Input_L</i>	125	<i>CR_2O</i>	100
<i>S</i>	30	<i>CR_3O</i>	140
<i>D</i>	45	<i>CR_4O</i>	130
<i>Tap_P</i>	500	<i>LO_2</i>	160
<i>CR_1S</i>	325	<i>LO_3</i>	200
<i>CR_2S</i>	210	<i>LO_4</i>	190
<i>CR_3S</i>	200	<i>Pad_W</i>	100
<i>CR_4S</i>	200	<i>CL_1</i>	170
<i>CL_2</i>	190	<i>CL_3</i>	200
<i>CL_4</i>	215		

width of 5  $\mu\text{m}$ . The length of the first four CPW resonators is 570  $\mu\text{m}$ , 560  $\mu\text{m}$ , 590  $\mu\text{m}$  and 580  $\mu\text{m}$ , respectively. The other physical dimensions are provided in Table 4.1.

This filter was fabricated by the MIT-Lincoln lab and measured using the Lakeshore Cryogenic Probe Station (Fig. 4.2-8) [51] in the CIRFE lab at the University of Waterloo. The probe calibration and measurement were carried out at 4K. A comparison between EM simulation and measurement results are given in Fig. 4.2-9, and a good agreement is observed. There are some factors that limit the agreement between the simulation and measurement results. As demonstrated in Fig. 4.2-3 (b), the process tolerance can also lead to a mismatch between the EM simulation and measurement results. Moreover, the dielectric properties of the  $\text{SiO}_2$  layers are assumed to be constants across all the frequency bands in the EM simulation. However, the material properties are frequency-dependent in practice. For future work, material properties will be characterized at millimeter wave frequencies.



Fig. 4.2 - 8. The fabricated filter was measured with a Lakeshore Cryogenic Probe station.

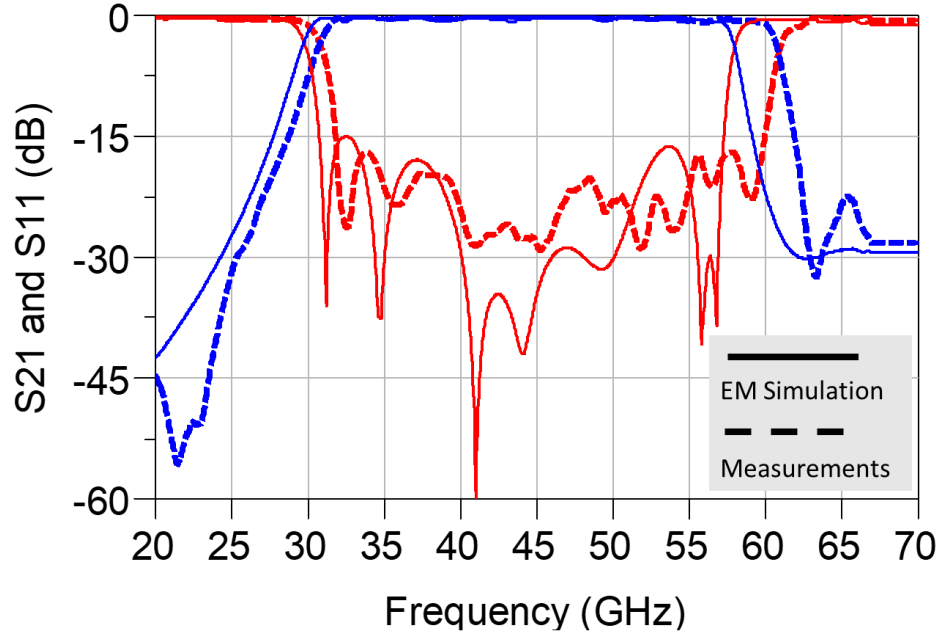


Fig. 4.2 - 9. The EM simulation and measurement results of the mm-Wave UWB bandpass filter.

## 4.3 Nb-Based mm-Wave Wideband Superconductor Diplexer

Figure 4.3-1 shows the top 2D layout view of the Nb-based mm-Wave wideband superconductor diplexer with the first channel passband from 25 GHz to 35 GHz and the second channel passband from 40 GHz to 50 GHz. The CPW signal lines are realized on the 1<sup>st</sup> Nb layer (M7). The ground planes of the CPW lines are realized on all the Nb layers and are connected using vias to satisfy the metal fill requirements of the MIT-LL 8-Nb-layer process. Crossovers of the channel filters are built on the 2<sup>nd</sup> Nb layer (M6). The same design procedures introduced in section 3.6 are used to develop this Nb-based diplexer. Figure 4.3-2 presents the EM simulation results for this diplexer.

A Lakeshore Cryogenic Probe Station is used to measure the fabricated triplexer at 4K. To measure the 3-port diplexer in the cryogenic RF probe station with only two RF probes, one port of the triplexer should be terminated to 50 OhmS when the other two ports are measured. A broadband matched load is needed for this approach. The lossy conductor layer R5 in the MIT-LL process can be used to develop the broadband matched load. In [11], a broadband matched load up to 40 GHz has been reported. As analyzed in [11], a meander lossy line with a floating metal plate underneath is used to cancel the parasitic reactance of the lossy line. For the current diplexer design and the

UWB triplexer which will be presented in the next section, a 50 Ohm load resistor from 10 GHz to 90 GHz is required. As shown in Fig. 4.3-3, the same meander lossy line structure is also used, but the floating metal plate employed in [11] is replaced with a ground plane built on layer M7. The modification helps to extend the performance of the matched load to 90 GHz, with a resistance of 50 OhmS and an almost zero reactance from 0-90 GHz. This 50 Ohm resistor design promises to be useful in a wide range of superconductor mm-Wave applications that require the use of 50 Ohm terminations.

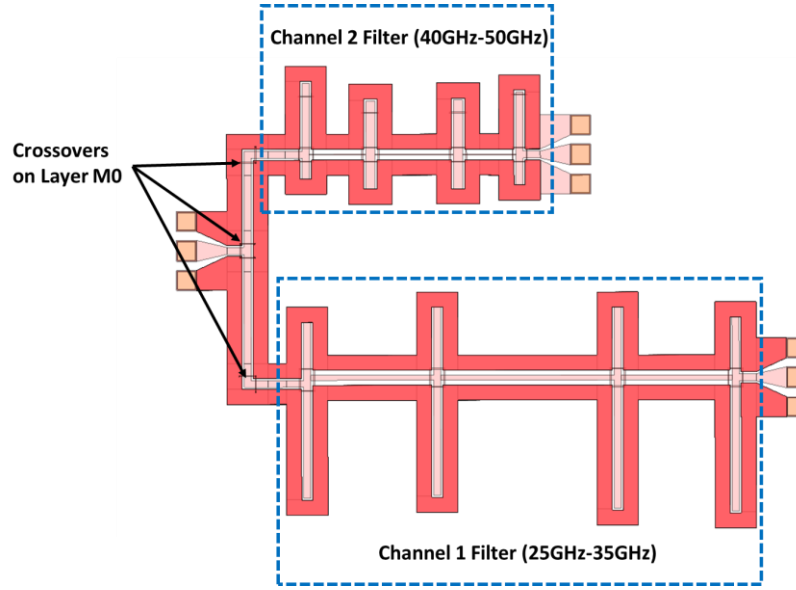


Fig. 4.3 - 1. The 2D layout of the designed mm-Wave wide band superconductor diplexer.

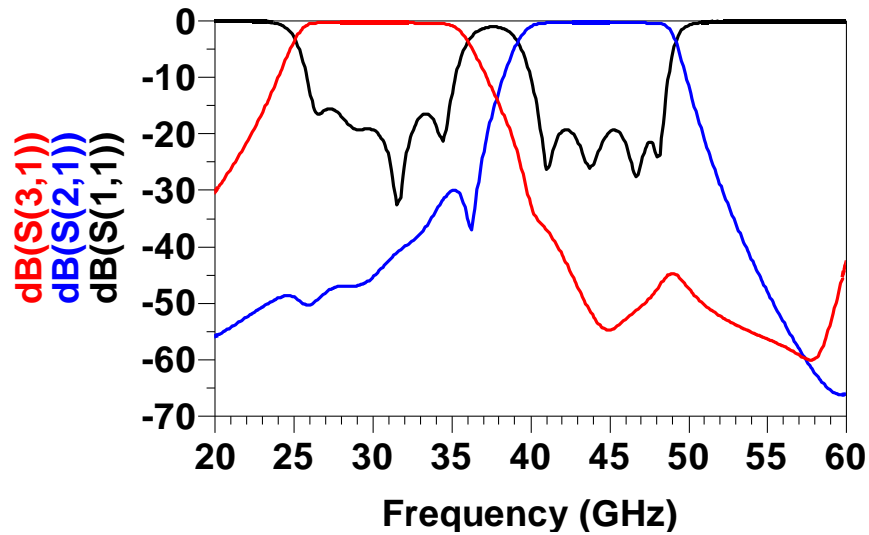


Fig. 4.3 - 2. The EM simulation results of the designed Nb-based mm-Wave wide band superconductor diplexer.

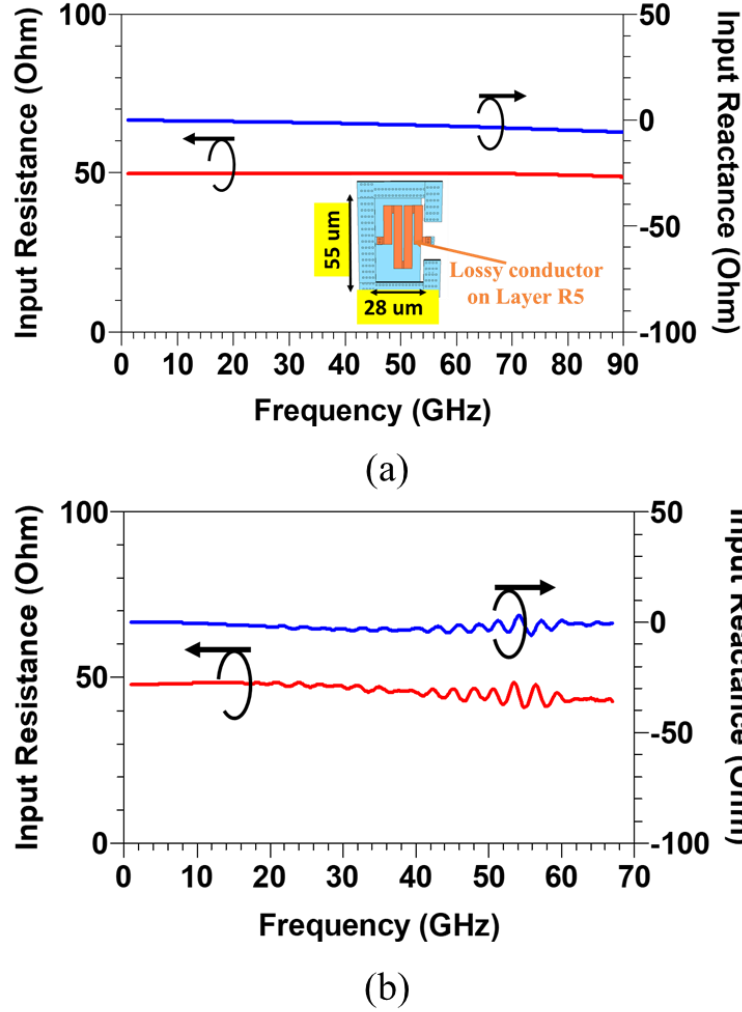
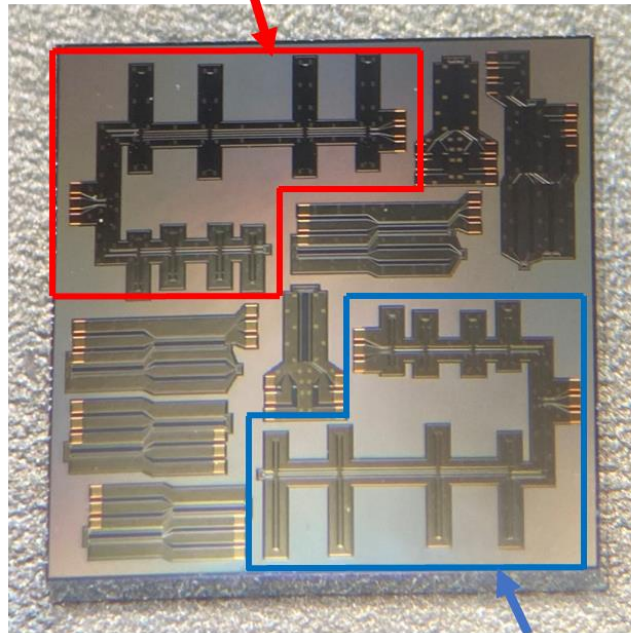


Fig. 4.3 - 3. (a) The EM simulation results, and (b) the measurement results of the broad band 50 Ohm matched load realized on layer R5.

Figure 4.3-4 shows photos of the fabricated diplexer measured by using a Lakeshore Cryogenic Probe Station with two RF probes at 4K. The measurement results are provided in Fig. 4.3-5. As can be seen, there are mismatches between the measurement results and the EM simulation results provided in Fig. 4.3-2. The frequency mismatch is mainly attributed to fabrication tolerance. One possible reason for higher insertion losses in the measurement results could be that the Nb chip was not cooled down enough. This can make parts of the Nb in the diplexer circuit operate as a normal conductor rather than a superconductor, and significant ohmic losses are then unexpectedly introduced. Issues related to the non-perfect cooling down process will be discussed in detail in Chapter 5.

**Channel 2 Filter (40GHz-50GHz)  
is terminated with a 50 Ohm load.**



**Channel 1 Filter (25GHz-35GHz)  
is terminated with a 50 Ohm load.**

Fig. 4.3 - 4. Photo of the fabricated Diplexer.

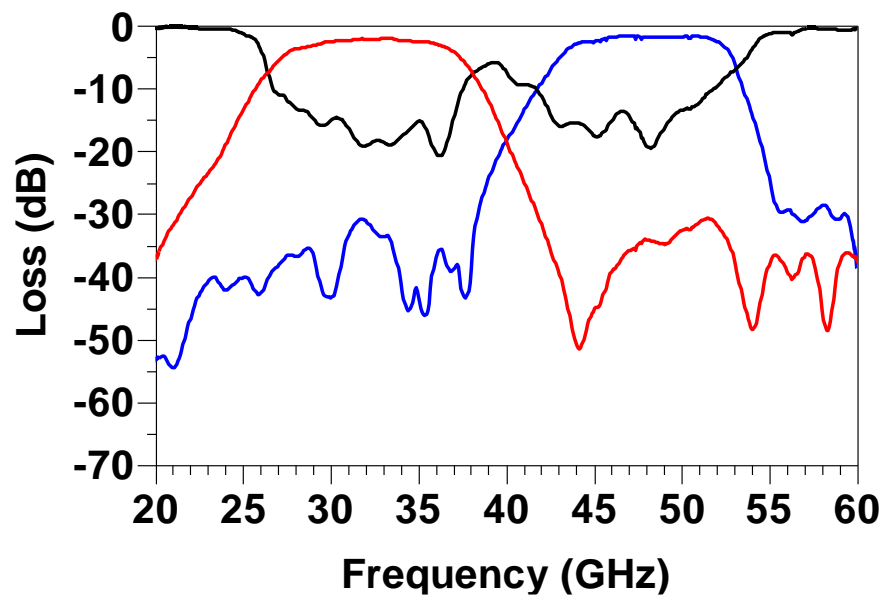


Fig. 4.3 - 5. Measurement results of the fabricated diplexer.



## 4.4 Nb-Based mm-Wave UWB Superconductor

### Contiguous Triplexer

In this section, a highly miniature mm-Wave UWB superconductor contiguous triplexer with an overall physical size of 2.5 mm x 3.6 mm (Fig. 4.4-1) is developed. The triplexer consists of three wideband bandpass filters with passbands of 20 GHz – 40 GHz, 40 GHz – 60 GHz, and 60 GHz – 80 GHz. The designed triplexer is fabricated with the MIT-LL using the 8-Nb-layer fabrication process.

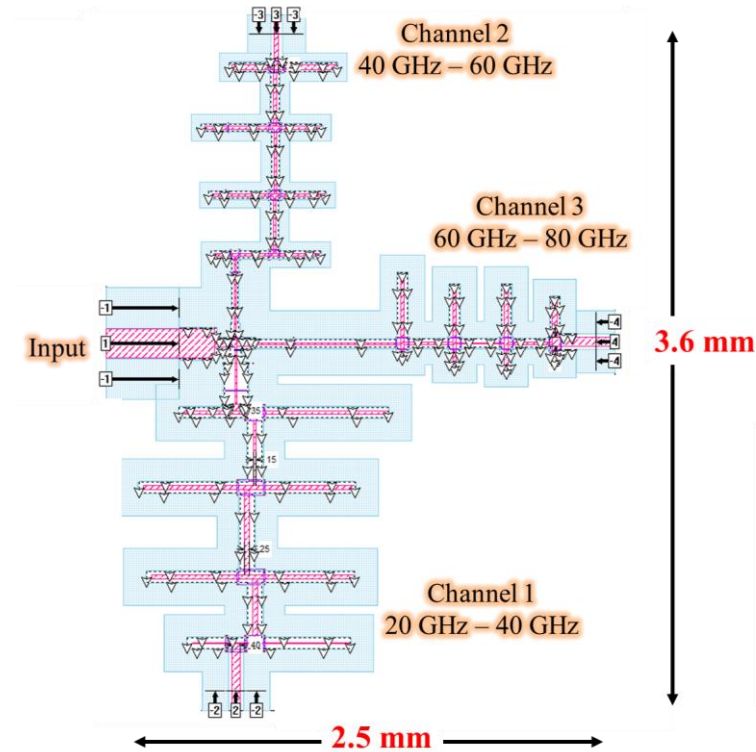


Fig. 4.4 - 1. The schematic of the mm-Wave UWB triplexer.

Figure 4.4-2 depicts the 3D layout of the triplexer. In this design, each channel of the triplexer has a four-pole CPW wideband bandpass filter. The CPW signal lines (shown in red in Fig. 4.4-2) are realized only on layer M7, while the CPW ground planes (shown in blue in Fig. 4.4-2) are built on all the niobium layers (M0 to M7) to meet the metal filling requirement for the fabrication process. They are connected together using vias (I0-I6) through the dielectric layers. The crossovers are built on layer M6 at a height of 200 nm and using SiO<sub>2</sub> to isolate each crossover from the CPW signal line. The short crossover height and the dielectric material guarantee sufficient capacitance loading to achieve a reduction in the physical size of the channel filter.

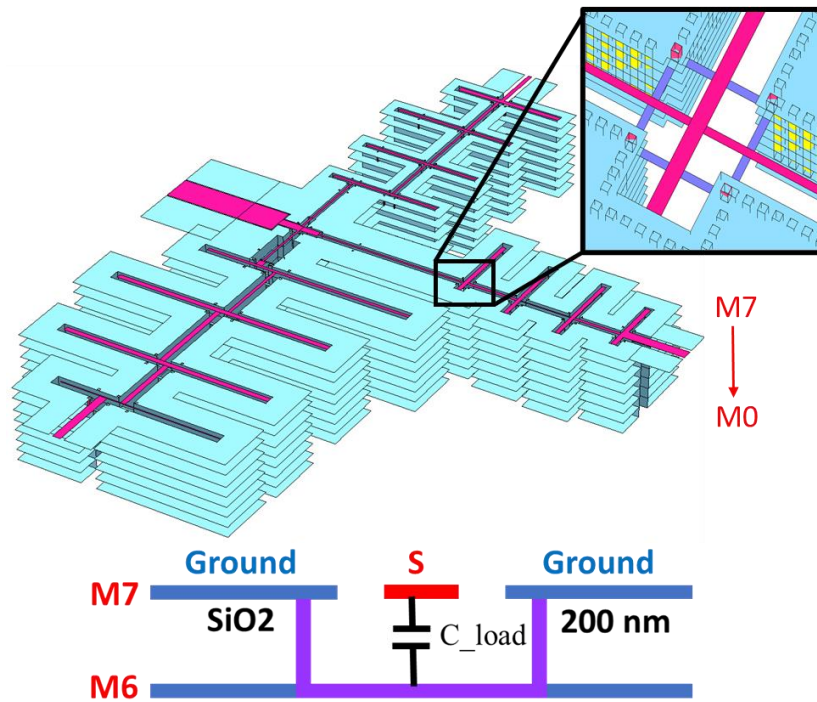


Fig. 4.4 - 2. The 3D layout of the triplexer. Crossovers are built on layer M6.

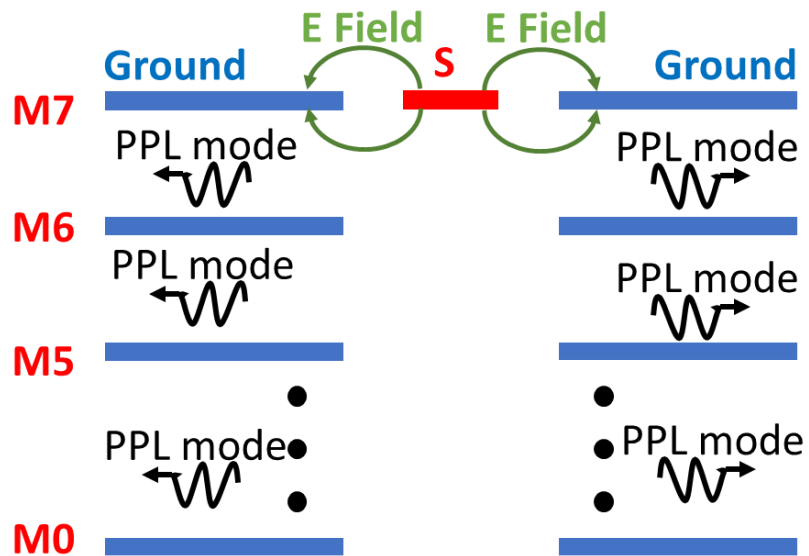


Fig. 4.4 - 3. Parasitic parallel-plate modes in between the CPW ground planes.



Since the CPW ground planes are built on all the Nb layers, this configuration supports not only the desired CPW mode (shown in green), but also parasitic parallel-plate (PPL) modes, as illustrated in Fig. 4.4-3. The fields of PPL modes resemble the parallel plate case and are concentrated in between the ground planes. At mm-Wave frequencies, the effects of the unexpected PPL modes are more pronounced. To eliminate the PPL modes, edge vias, shown in yellow in Fig. 4.4-4, are used. Using edge vias slightly increases the capacitance between the CPW single line and ground planes, which results in a further reduction in size.

Conventionally, to design a triplexer, the circuit model is synthesized [9] first, as shown in Fig. 4.4-5. Next, each block in the circuit model is mapped into its corresponding physical layout, respectively, after which all the physical layout blocks are joined together and full EM simulation and optimization are finally applied. This conventional method, however, works best only for narrowband triplexers designed at low frequencies.

There are several reasons why the conventional method does not work well for mm-Wave UWB triplexer design cases. First, the filter coupling matrix in the circuit mode does not count for the dispersion effect for wideband filters. Secondly, crosstalks due to radiation between each channel filter in the physical mode exist in practice, as shown in Fig. 4.4-6. It is very difficult to accurately model those crosstalks in the circuit model. Since multi-layer structures and a large amount of edge vias are used in this design, full EM simulation for the whole physical structure over an ultra-wide frequency band requires massive computational resources. Thus, EM-based optimization is

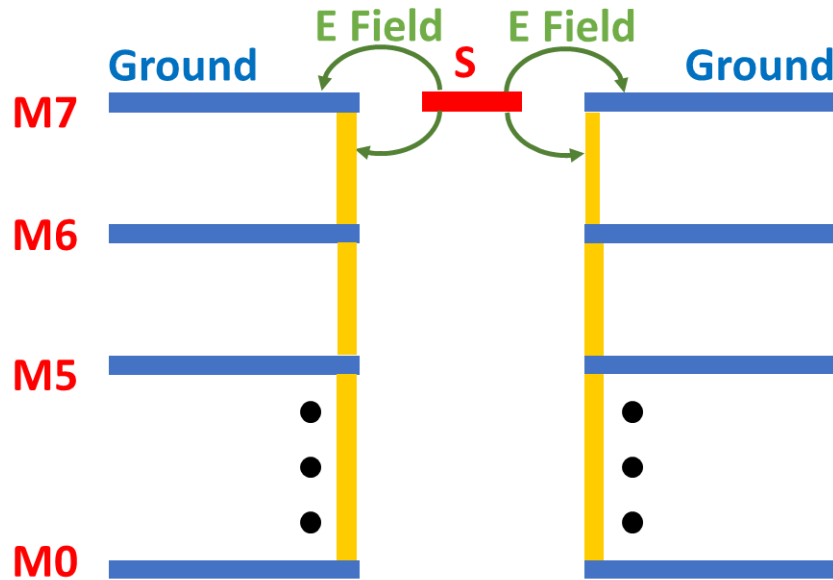


Fig. 4.4 - 4. Edge vias are used to suppress the parasitic parallel-plate modes.

impossible with reasonable computational time and resources. This limitation is one of the toughest challenges in designing wideband filters and multiplexers.

Moreover, the circuit mode does not count for the higher propagation modes (harmonics) of the physical filter. Figure 4.4-7 shows the responses of circuit and physical models in an ultra-wideband bandpass filter. As can be seen, the physical model responses match those of the circuit

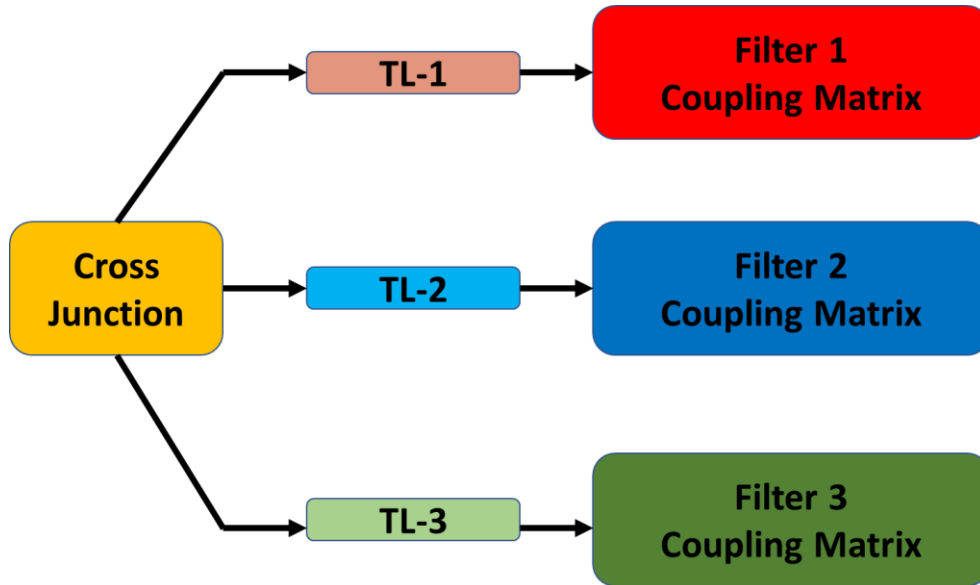


Fig. 4.4 - 5. The circuit model of the triplexer includes the filter coupling matrices.

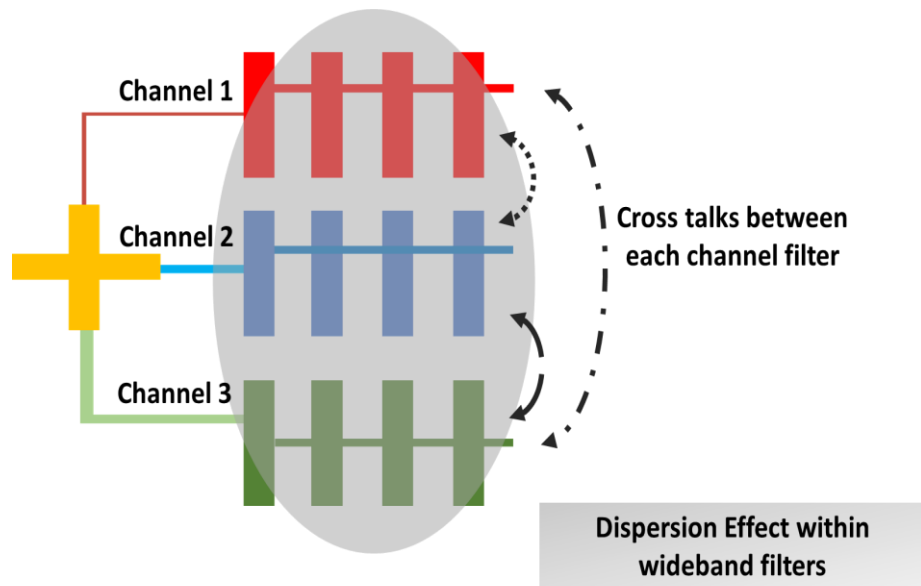


Fig. 4.4 - 6. Dispersion effect and cross talks between channel filters exist in the physical model of the ultra-wide band triplexer.

model very well within the passband. However, the higher rejection band responses for those same two models are totally different. This is a very important consideration for ultra-wideband multiplexer design. Thus, the EM performance of the stopband of the 1<sup>st</sup> channel needs be carefully investigated to circumvent its interference with the passbands of the 2<sup>nd</sup> and 3<sup>rd</sup> channel filters.

To overcome all of the issues mentioned above, a hybrid model simulation is used to design mm-Wave ultra-wideband triplexers. The major steps of the design procedures are shown in Fig. 4.4-8. The design starts with the synthesised circuit model for the triplexer as shown in the 1<sup>st</sup> plot of Fig. 4.4-8. Then, the cross-junction is replaced with its corresponding physical structural model. A hybrid model combining physical structures and circuit mode blocks is obtained, as shown in the 2<sup>nd</sup> plot of Fig. 4.4-8. Next, only circuit model blocks in this hybrid model are optimized to meet the design requirements. After that, in the 3<sup>rd</sup> plot, the circuit model of the 1<sup>st</sup> channel is replaced by its physical model. Only the circuit model blocks of the 2<sup>nd</sup> and 3<sup>rd</sup> channels are optimized to ensure the responses meet the design requirements. As shown in the 4<sup>th</sup> and 5<sup>th</sup> plots of Fig. 4.4-8, the same procedure is repeated until all physical structure models replace their circuit model blocks.

A comprehensive design procedure flow chart with more details is provided in Fig. 4.4-9. It should be noted that the physical structures of the 1<sup>st</sup> channel filter along with junction and the transmission lines to the channels are developed first, since the higher order harmonics of the 1<sup>st</sup>

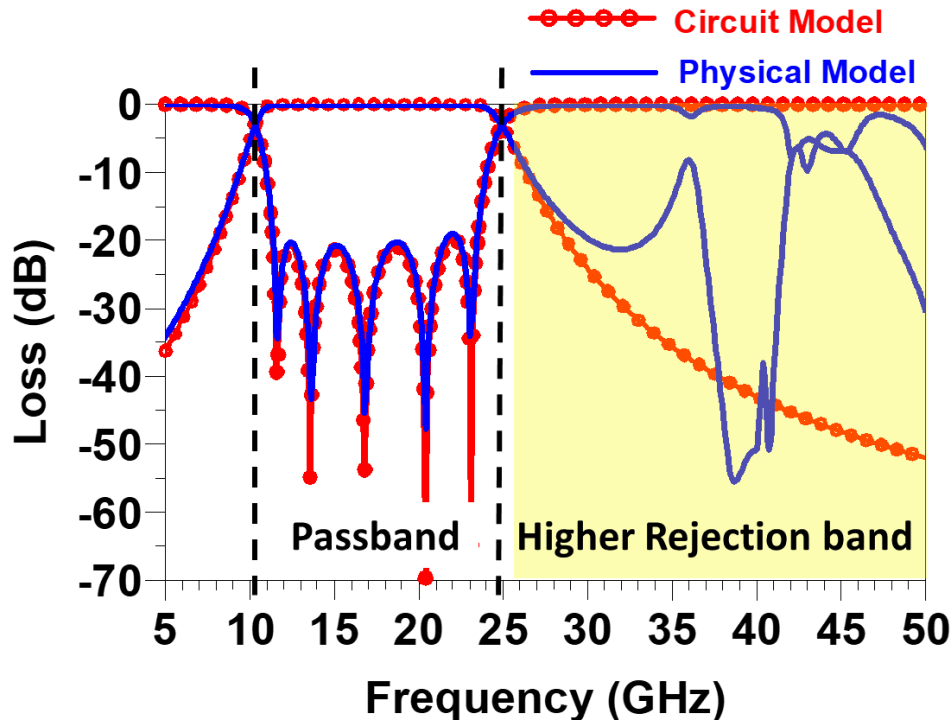


Fig. 4.4 - 7. The circuit mode does not take into account the higher propagation modes (harmonics) of the physical filter.

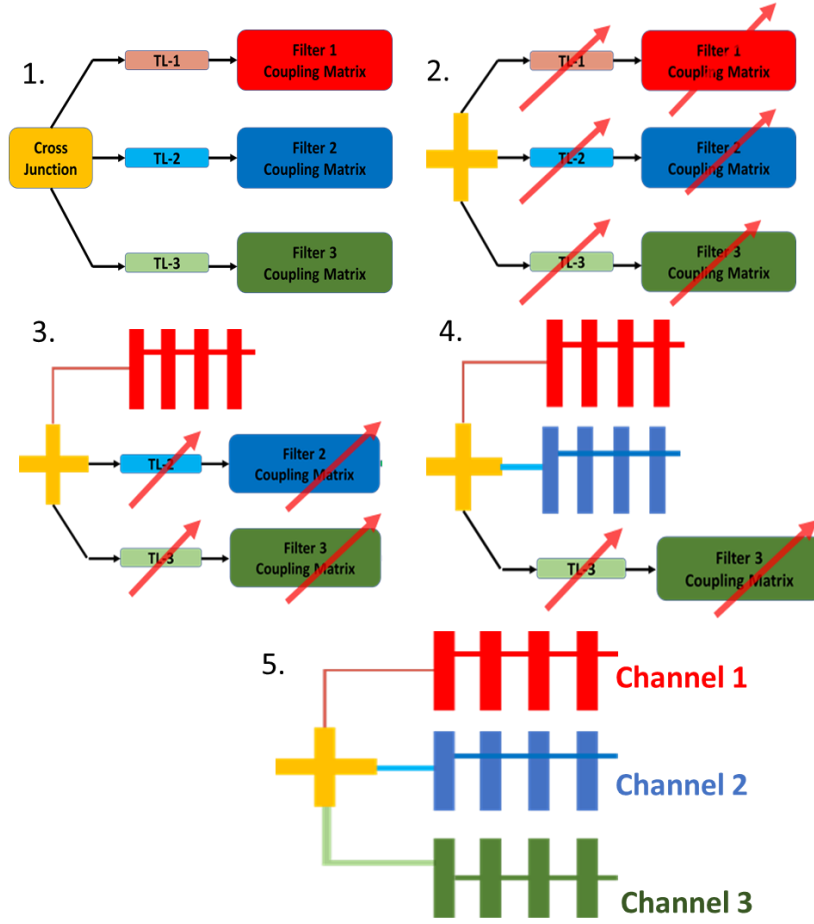


Fig. 4.4 - 8. Major steps of the design procedure for the proposed UWB triplexer.

channel need to be pushed away from the passbands of the 2<sup>nd</sup> and 3<sup>rd</sup> channels. Sometimes, to suppress the harmonics, it is necessary to have an extra lowpass filter between the 1<sup>st</sup> channel filter and the cross-junction. For this case, the circuit model at the very beginning step needs to be re-developed.

While using the hybrid model simulations shown in Fig. 4.4-8, optimization is only applied to the circuit model blocks. The PII method introduced in Chapter 3 was used to develop the physical structures of the channel filters from the circuit models. During each step, if optimizing the circuit model blocks cannot meet the design requirements, only the physical structures obtained from the previous step need to be redesigned. By following the design procedures, the design efficiency is improved significantly, since the EM-based optimizations required by the conventional design method in [9] is not used. The EM simulation results of the designed triplexer are shown in Fig. 4.4-10.

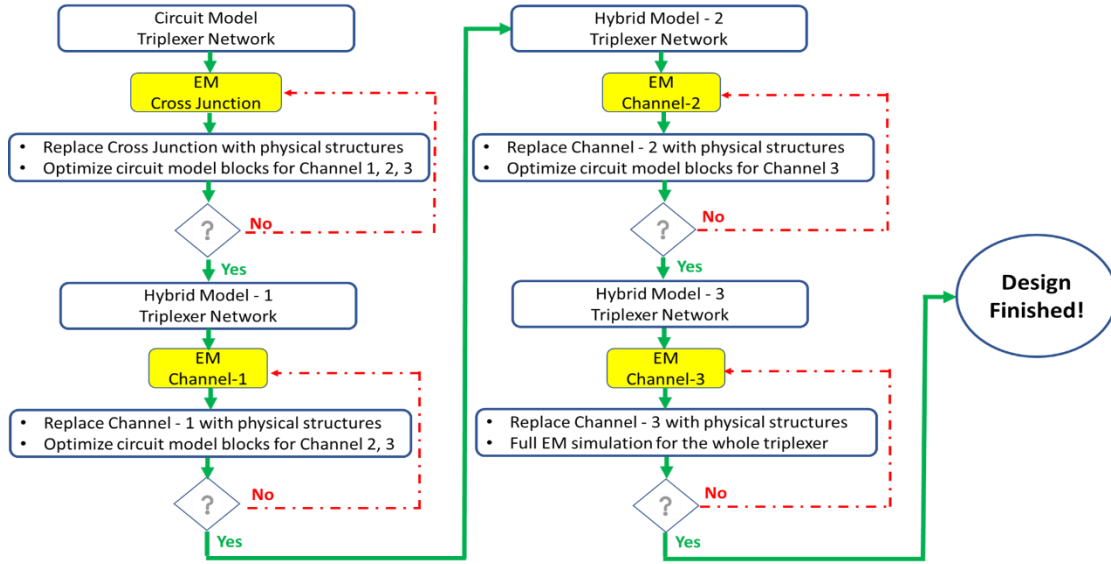


Fig. 4.4 - 9. Flow chart of the hybrid model design procedures.

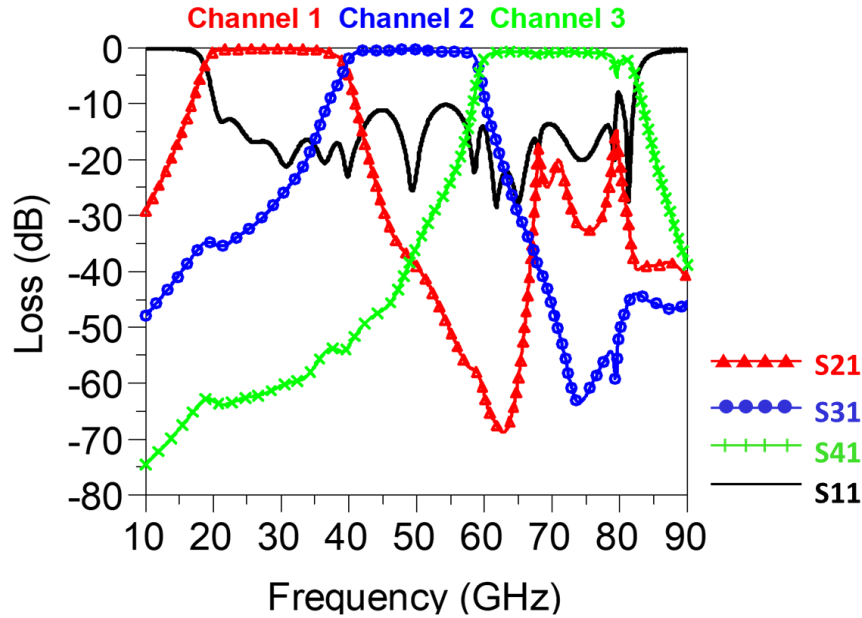


Fig. 4.4 - 10. The EM simulation results of the mm-Wave ultra-wide band contiguous triplexer.

A Lakeshore Cryogenic Probe Station is used to measure the fabricated triplexer at 4K (Fig. 4.4-11), with the measurement results for the first two channels of the triplexer provided in Fig. 4.4-12. In comparison with the EM simulation results, a good agreement is observed. It should be noted that our Lakeshore Cryogenic Probe Station is designed to work only up to 40 GHz, and the PNA is designed to work only up to 67 GHz. This explains why we presented only measured results for the first two channels. It also explains the reason for the presence of the ripples in the measured results of the 2<sup>nd</sup> channel in Fig. 4.4-12.

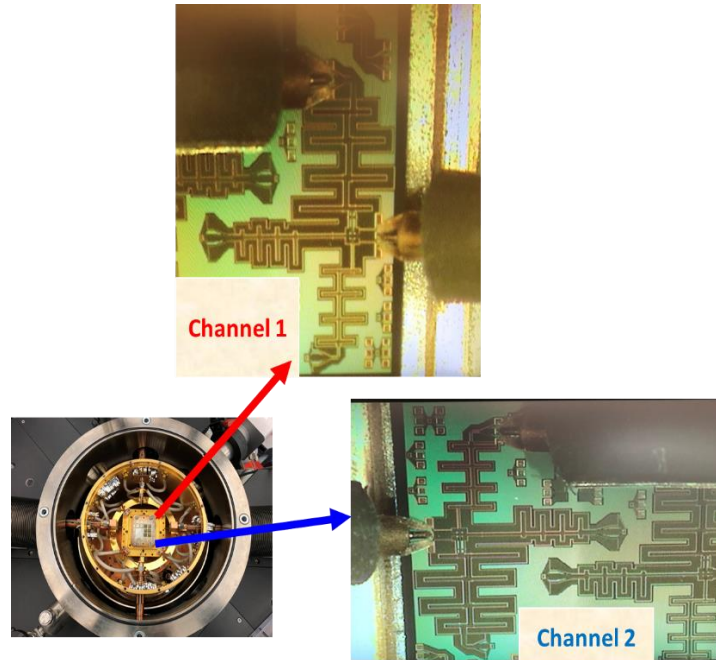


Fig. 4.4 - 11. The fabricated triplexer was measured with a Lakeshore Cryogenic Probe station.

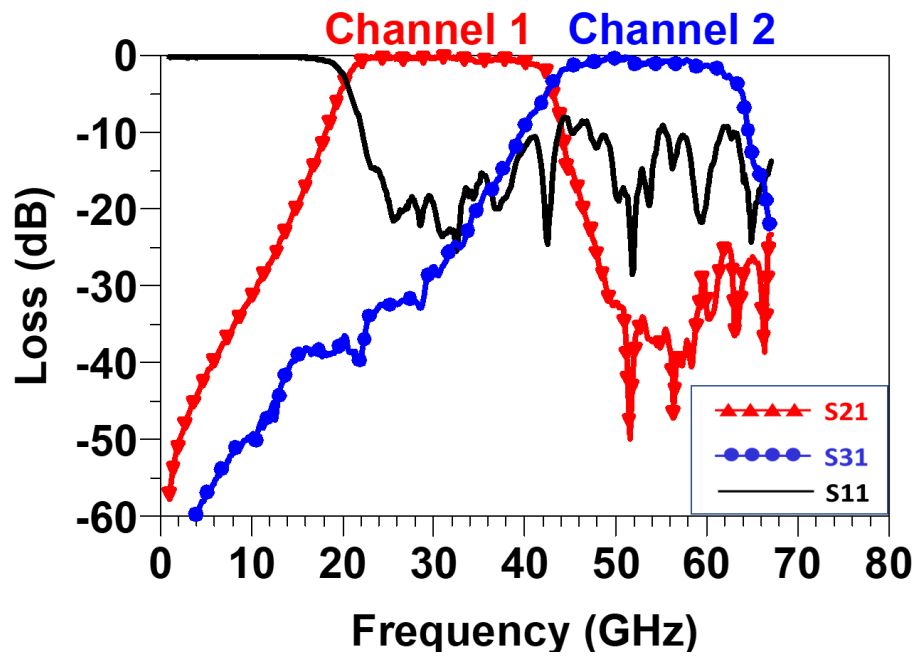


Fig. 4.4 - 12. Measurement results of the first two channels of the fabricated triplexer.

## 4.5 Integration on Multi-Chip Module (MCM)

### Substrate with 1 mm Millimeter-wave Connectors

In the previous sections, a mm-Wave UWB superconductor contiguous triplexer with a coverage from 20 GHz to 80 GHz was designed, fabricated, and tested using a cryogenic RF probe station. The designed triplexer has a miniature physical size, which allows it to realize the entire SME RF front-end shown in Fig. 4.1-1 on a single chip. This section will explore the possibility of integrating the mm-Wave triplexer on an MCM substrate using flip-chip technology and interfacing it with commercially available 1 mm RF connectors for testing. This helps in digital receiver applications where the superconductor ADCs and the RF front-end components are in separate

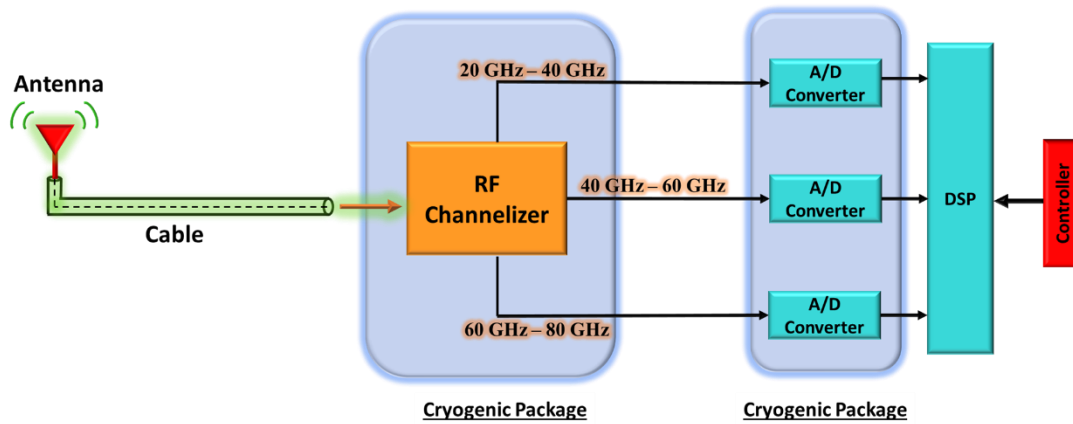


Fig. 4.5 - 1. The SME chip can be connected to an antenna outside the cryogenic package via an RF cable.

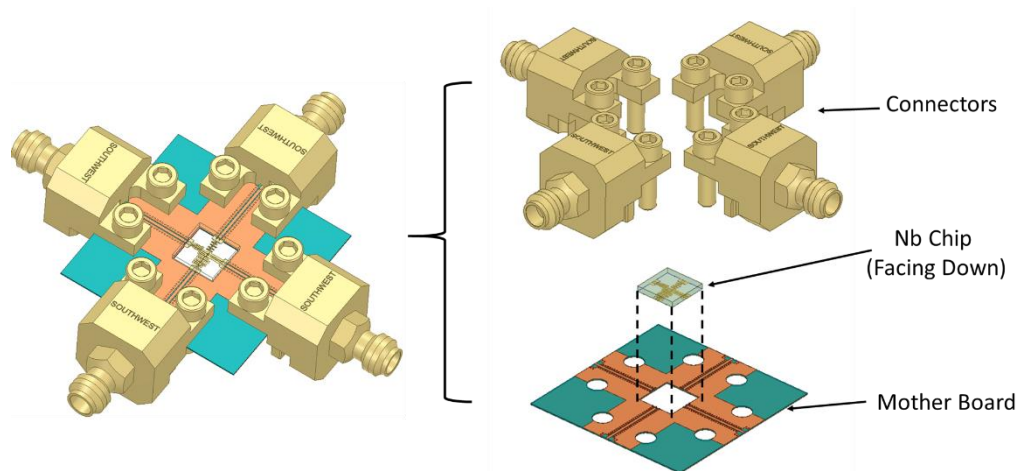


Fig. 4.5 - 2. The triplexer is realized on a 4.7 mm x 4.7 mm Nb chip. The Nb chip is assembled on a mother board using the flip-chip technology. Four commercially available RF connectors are assembled with the mother board.

cryogenic packages, as shown in Fig. 4.5.1. The work in this section mainly focusses on exploring and developing the assembled circuit depicted in Fig. 4.5-2.

In Fig. 4.5-2, the triplexer is realized on a 4.7 mm x 4.7 mm Nb chip. The four end-launch 1mm RF connectors operating from DC to 100 GHz are commercially available from Southwest Microwave Inc.; the part number is 2492-04A-9 [52]. Conventionally, the wire bonding technology is very popular for integrating chips to motherboards for low-frequency applications. However, such bonding wires have electrically large lengths, which introduce severe parasitic inductance for mm-Wave applications [53]. For example, as shown in Fig. 4.5-4, the bonding wires need to have a length greater than 1 mm to be connected to the 635  $\mu\text{m}$  thick Nb chip on the MCM substrate.

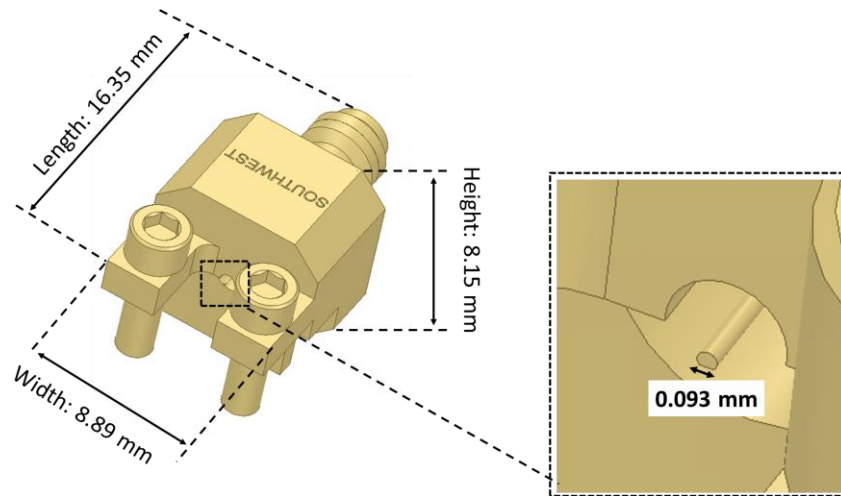


Fig. 4.5 - 3. The dimensions of the end lunch RF connector operating from DC to 110 GHz. More detailed dimensions of this connector can be found at [52].

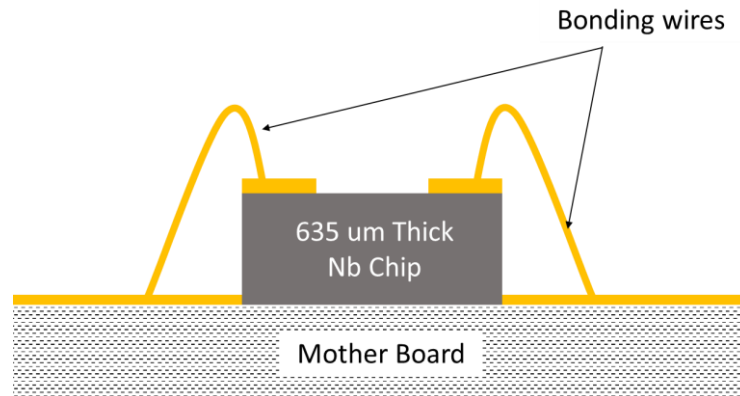


Fig. 4.5 - 4. Bonding the Nb chip on the mother board by using the wire bonding technology. The diagram is not to scale.



The flip-chip technology is the optimum integration technology for millimeter-wave MCM integration.

The flip-chip technology for mm-Wave applications has been extensively studied in [54]-[58]. The most recent results [58] demonstrate that the flip-chip interconnection can cover the frequency band from DC to 500 GHz. Figure 4.5-6 shows the structure of the flip-chip transition. On the Nb chip, a 50 Ohm CPW line is constructed at the M8 layer of the MIT-LL8 Nb layer process, with a

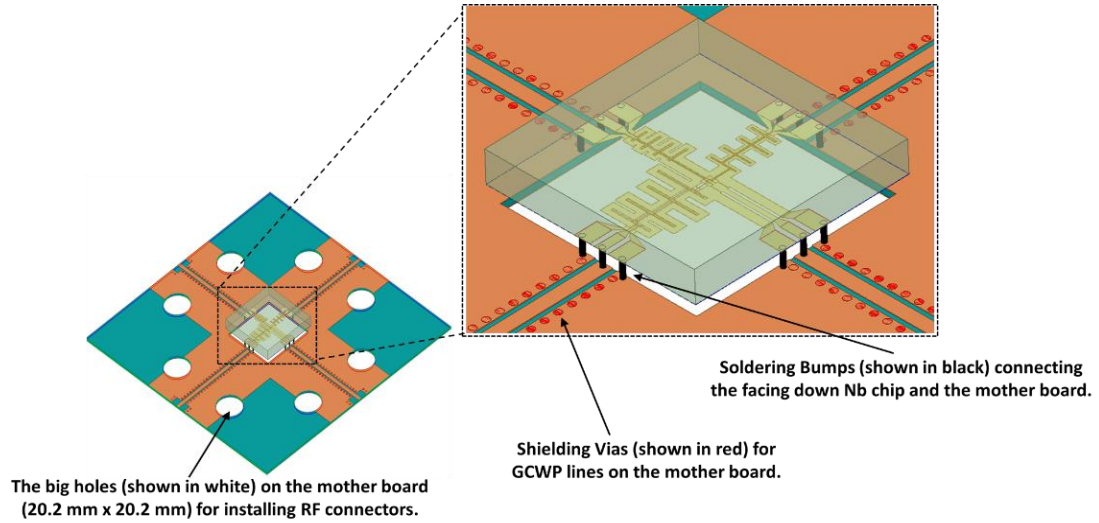


Fig. 4.5 - 5. Bonding the triplexer Nb chip on the mother board by using the flip-chip technology. The diagram is not to scale.

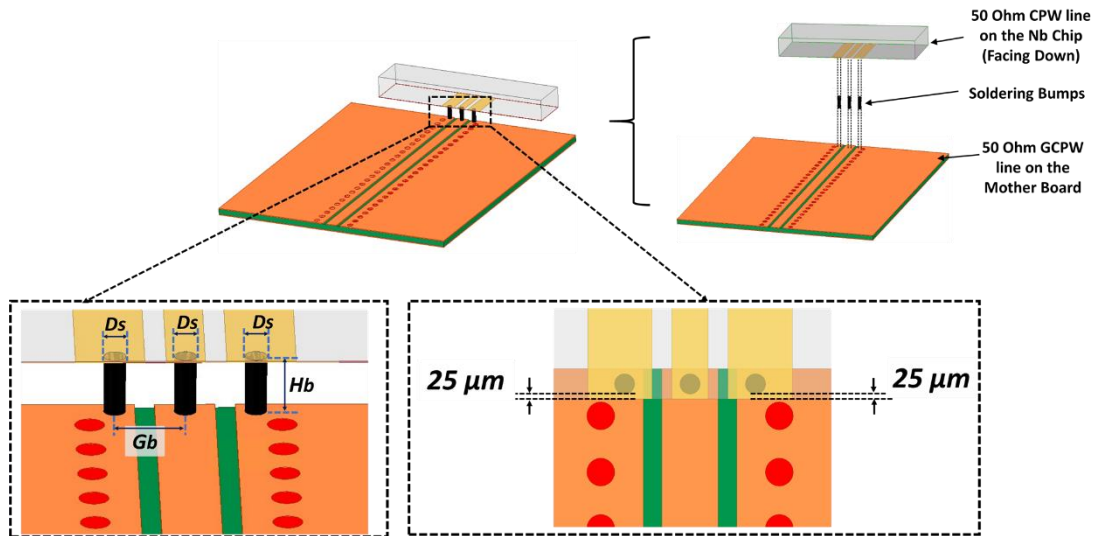


Fig. 4.5 - 6. The structure of the flip-chip transition. The diagram is not to scale.

signal line width of 147  $\mu\text{m}$ , a gap width of 106  $\mu\text{m}$ , and a ground plan width of 344  $\mu\text{m}$ . A 10-mil thick RT/duroid® 5880 with a half-ounce of copper on both sides is used as the MCM substrate. The 50 Ohm GCPW line on the MCM substrate has a signal line width of 300  $\mu\text{m}$ , a gap width of 100  $\mu\text{m}$ , a shielding vias diameter of 150  $\mu\text{m}$ , and a via-to-via (center) distance of 300  $\mu\text{m}$ . The soldering bumps are modeled as conductive cylinders with a conductivity of  $8.25\text{e}^6$  siemens/m [53].

The EM simulation was performed with  $D_s$  and  $H_b$  equal to 50  $\mu\text{m}$  and  $G_b$  equal to 350  $\mu\text{m}$  as the starting point. These bumps are very typical in size and can be easily fabricated by using any type of soldering manufacturing processes [59]. Figure 4.5-7 presents the EM simulation results. Further in Figure 4.5-7, when the operating frequency exceeds 74 GHz, the return loss level is higher than -20 dB. When the two 50 Ohm transmission lines are interconnected by soldering bumps, unwanted parasitic reactance will be inserted into the circuit. Referring to [58], the flip-

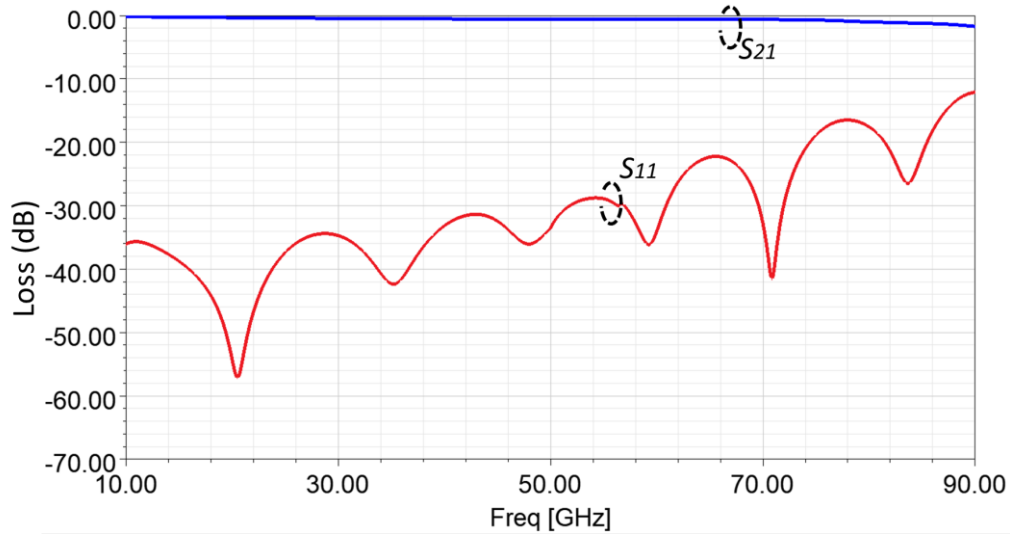


Fig. 4.5 - 7. The EM simulation result of the flip-chip transition structure shown in Fig. 4.5-6.  $D_s = H_b = 50 \mu\text{m}$ .  $G_b = 350 \mu\text{m}$ . The length of the 50 Ohm CPW line on the Nb chip is 494  $\mu\text{m}$ . The length of the 50 Ohm GCPW line on the mother board is 7.9 mm.

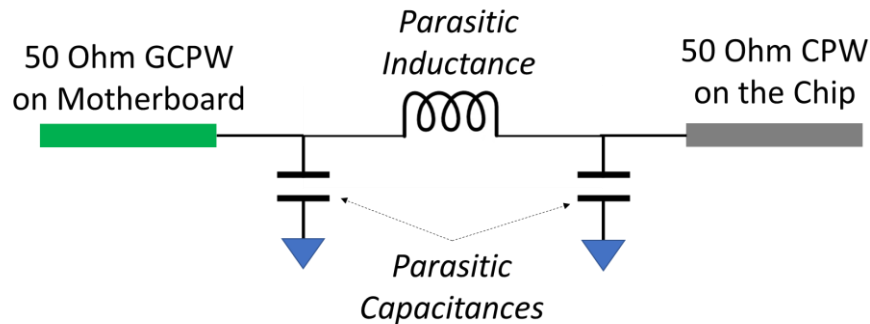


Fig. 4.5 - 8. The basic equivalent circuit model for the flip-chip interconnection with the loss ignored. [58]

chip interconnection can be modeled as the parasitic inductance and parasitic capacitances between the two 50 Ohm transmission lines, as shown in Fig. 4.5-8. The values of the parasitic reactance usually scale with the dimensions of the soldering bumps, and the parasitic inductance and capacitance can be managed to cancel each other by dimensioning the soldering bumps. Moreover, and as illustrated in Fig. 4.5-9 and Fig. 4.5-10, the simulation results shown in Fig. 4.5-7 can be improved with a return loss level below -20 dB from 10 GHz to 86 GHz by either adjusting the height or the diameter of the bumps, respectively. The flip-chip structures shown in Fig. 4.5-6 are

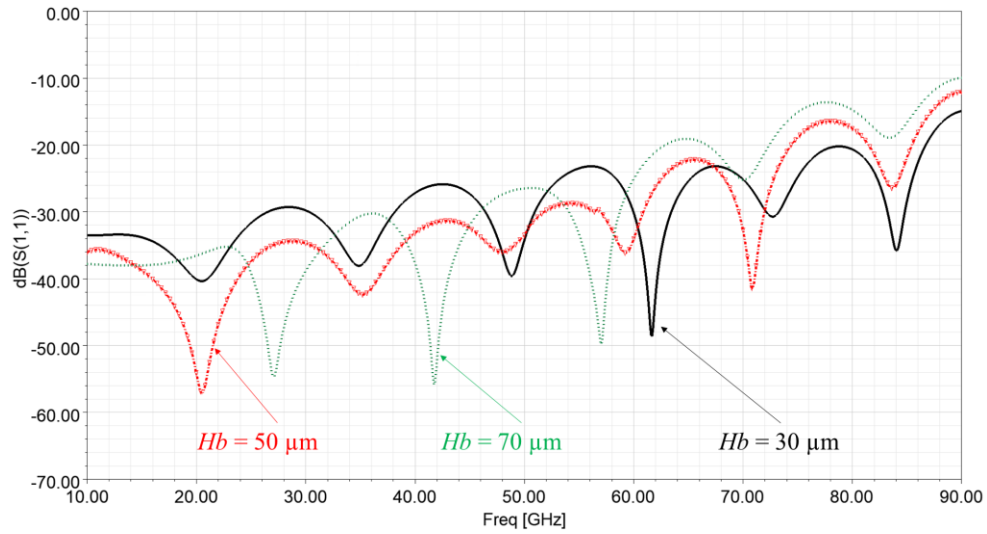


Fig. 4.5 - 9. The EM simulation results of the flip-chip transition structure shown in Fig. 4.5-6 with the height of the bumps swept. All the three bumps have the identical diameter of 50  $\mu\text{m}$ . The length of the 50 Ohm CPW line on the Nb chip is 494  $\mu\text{m}$ . The length of the 50 Ohm GCPW line on the mother board is 7.9 mm.

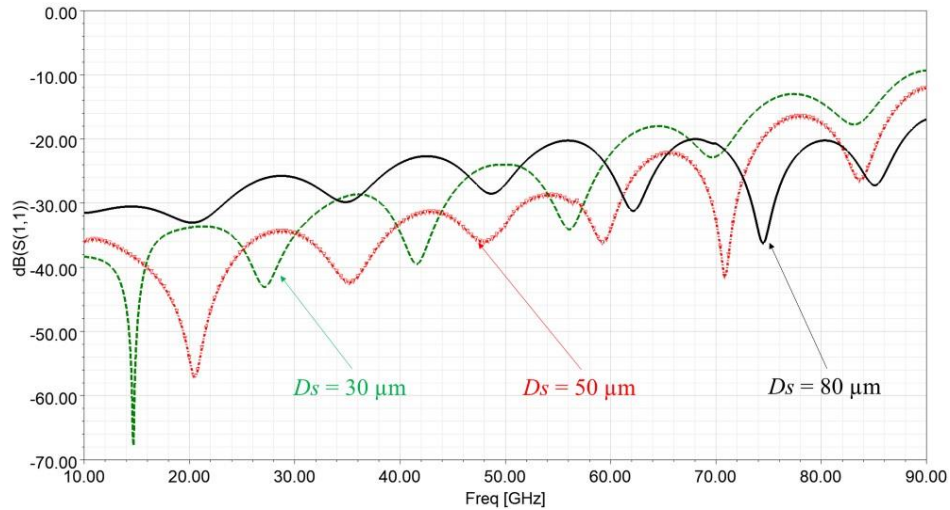


Fig. 4.5 - 10. The EM simulation results of the flip-chip transition structure shown in Fig. 4.5-6 with the diameters of the bumps swept. The height of the bumps is 50  $\mu\text{m}$ . The length of the 50 Ohm CPW line on the Nb chip is 494  $\mu\text{m}$ . The length of the 50 Ohm GCPW line on the mother board is 7.9 mm.

then connected to the connector, with the simulation given in Fig. 4.5-11. The encrypted HFSS model of the RF connector is provided by Southwest Microwave Inc. Finally, the structure depicted in Fig. 4.5-11 is connected to each port of the Nb triplexer chip (Fig. 4.5-2), and the EM simulation results (Fig. 4.5-12) indicate good RF performance.

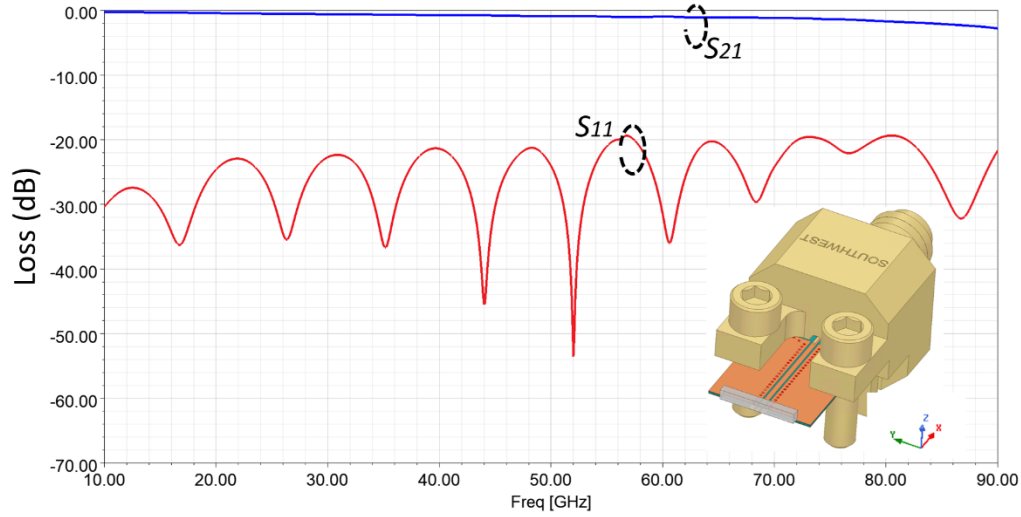


Fig. 4.5 - 11. The EM simulation results of the flip-chip transition structure shown in Fig. 4.5-6 connected with the connector. The height of the bumps is 80  $\mu\text{m}$  and the diameter of the bumps is 50  $\mu\text{m}$ . The length of the 50 Ohm CPW line on the Nb chip is 494  $\mu\text{m}$ . The length of the 50 Ohm GCPW line on the mother board is 7.9 mm. The encrypted HFSS model of the connector is provided by Southwest Microwave Inc.

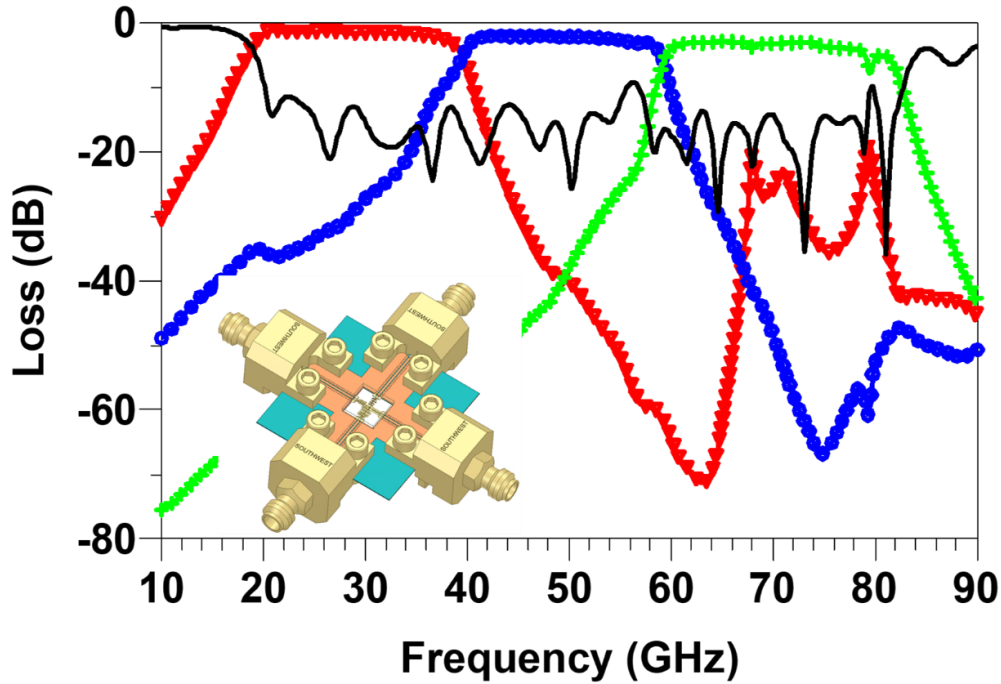


Fig. 4.5 - 12. The EM simulation results of the Nb-based triplexer. The Nb chip is mounted on the motherboard by using the flip-chip technology and RF connectors are assembled with the mother board.



Fig. 4.5 - 13. The photo of the triplexer chip mounted on an MCM substrate using flip-chip technology interfaced with 1 mm mm-Wave connectors.

Figure 4.5-13 illustrates the photo of the triplexer chip mounted on an MCM substrate using flip-chip technology interfaced with 1 mm mm-Wave connectors. In this design, the thickness of the MCM substrate is 10 mil, and thus it is very soft. Since the 50 Ohm transmission lines on the MCM substrate are realized as grounded-CPW lines, a thick aluminum plate can be attached on the backside of the substrate to improve stiffness and thermal conductivity without affecting RF performance. Another consideration is the mechanical stability of the flip-chip structure used in this design. The Nb chip in the current design is connected to the motherboard by using twelve bumps. At room temperature, the mechanical stability of the soldering bumps is not a concern. However, the Nb chip will need to be cooled down to a cryogenic temperature close to absolute zero. In the cryogenic case, the mechanical stability and thermal conductivity of the soldering bumps could become a potential concern. One possible solution is applying insulating adhesive pastes with good thermal conductivity under the four corners of the Nb chip, so that both the mechanical stability and thermal conductivity can be improved.

# **Chapter 5**

## **Miniature Ultra-Wideband Superconductor Filters with Interference Cancelation**

In order to having very low surface resistance, superconductors must operate below a certain critical temperature, magnetic field, and current for the materials to remain in the superconducting state. Film resistance changes as the RF/DC current approaches the critical current. In [60], a unique behaviour in a spiral superconductor inductor was observed when operating at high RF power. That led to the development of a power limiter [60]. In this chapter, we observe the same superconductor spiral inductor behaviour through the use of a high DC current. The concept is used to realize a switchable multiband band reject filter that can be switched from one state to another by a DC current. We integrate the band reject filters with a UWB filter for interference cancelation. It is important to have such interference cancelation capability, since operating on high power even at just a few milliwatts can damage the superconductor ADC. In this chapter, we also present a miniature Nb-based UWB triple-mode filter and very wideband couplers, which are needed to monitor and detect the interference signal.

### **5.1 Nb-Based Tunable Band Reject Filters**

Spiral inductors are employed in a wide range of microwave applications [61]-[63]. It is well-known that as the frequency of operation increases the spiral inductor resonates, the inductor performs as a capacitor when operating beyond its self-resonance frequency. This section demonstrates a unique behaviour of spiral inductors that are designed intentionally with a large parasitic capacitance. Such a spiral inductor performs as an inductor if it is made of high conductivity metals and as a capacitor if it is made of low conductivity metals, regardless of the frequency of operation, as long as certain conditions are met. Thus, using a mechanism that switches the conductivity of the metal strips from high value to low value allows changing the behaviour of the spiral structure from an inductor to a capacitor.

The concept was implemented in [60] to realize RF power limiters. In this section, the concept is applied to realize a switched tunable band reject superconductor filter, by controlling the conductivity of the metal strips forming the spiral inductor using a DC current. This section demonstrates a tunable band reject filter consisting of a CPW line capacitively coupled to three L-C resonators operating at three different frequencies. All of the elements are made of Nb operating at a temperature of 4K, i.e., operating in the superconducting state. Figure 5.1-1 shows a schematic of the tunable band reject filter. The inductors are connected to bias pads to allow the DC current to flow through the inductor. When the DC current exceeds the superconductor's critical current of Nb, the conductivity of the metals strips switches from very high conductivity to low conductivity close to the conductivity of Nb at room temperature.

At a zero DC bias current, the spiral inductor performs as an inductor and the shunt branch elements perform as a resonator. On the other hand, with the application of a DC current, the inductor performs as a capacitor, eliminating the resonance behaviour of the shunt branch. The

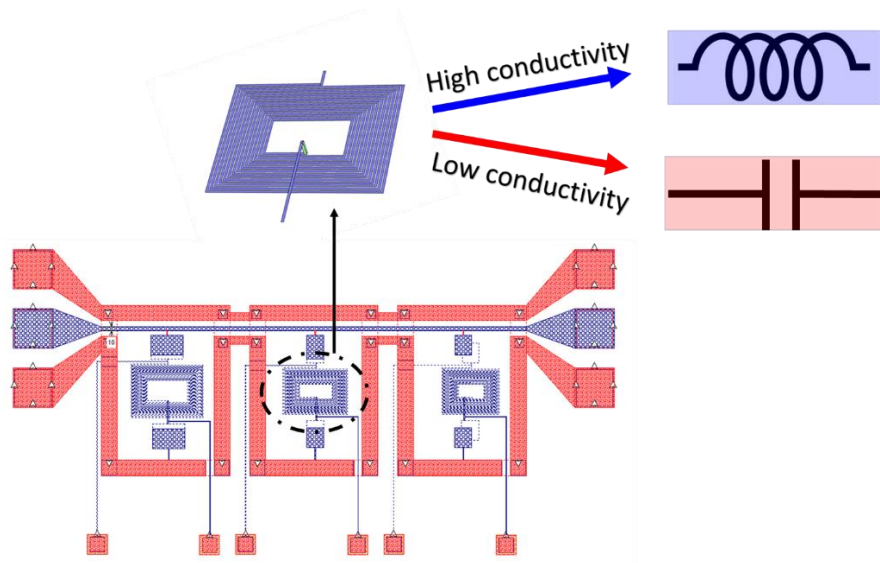


Fig. 5.1 - 1. The schematic of the tunable band reject filter circuit.

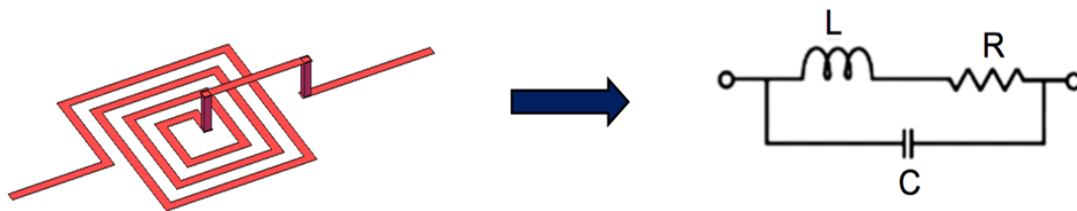


Fig. 5.1 - 2. Equivalent circuit model of a lumped spiral inductor.



design allows for the control of individual spiral inductors, thus further allowing for a multiple state band reject filter to realize rejection or non-rejection at any of the three bands simultaneously. The simulated and measured results for the switched band reject filter are presented demonstrating the validity of the concept.

Figure 5.1-2 depicts the equivalent circuit model of a lumped spiral inductor. The resistor represents the losses of the inductor, while the parallel capacitor represents the parasitic capacitance. It can be readily shown that the imaginary part of the impedance of the model illustrated in Fig. 5.1-2 is given by:

$$\text{Imag}(Z_{\text{Spiral}}) = \frac{\omega L \left(1 - C \frac{R^2}{L}\right) - \omega^3 L^2 C}{(1 - \omega^2 LC)^2 + \omega^2 C^2 R^2} \quad (5.1)$$

where  $\omega$  is the angular frequency. Moreover, it can be seen from Equation (5.1) that the imaginary part of  $Z_{\text{Spiral}}$  is negative (i.e., the inductor performs as a capacitor) when:

$$R^2 > \frac{L}{C} \quad (5.2)$$

It is interesting to note that the imaginary part of Equation (5.1) becomes negative regardless of the frequency of operation as long as the condition given by Equation (5.2) is satisfied. If both the parasitic capacitance  $C$  and  $R$  are high enough to satisfy Equation (5.2), the input impedance of the inductor yields a negative imaginary part similar to that of a capacitor. Thus, the physical dimensions of the spiral structure need to be selected properly to satisfy the condition given in Equation (5.2). Figure 5.1-3 shows two Nb spiral structures with different physical dimensions. Design 1 in Fig. 5.1-3 has a narrower conductor width, small gaps between the metal traces and more turns (i.e., a longer total length) than Design 2. Figure 5.1-4 shows the Sonnet EM simulation results of those two designs, assuming a lossless conductor and a finite conductivity equal to the Nb room temperature conductivity of  $6.5 \times 10^6$  S/m. Both designs behave as an inductor for the lossless case; however, the spiral inductor of Design 1 performs as a capacitor when assuming finite conductivity, while the spiral inductor of Design 2 operates as an inductor when assuming finite conductivity.



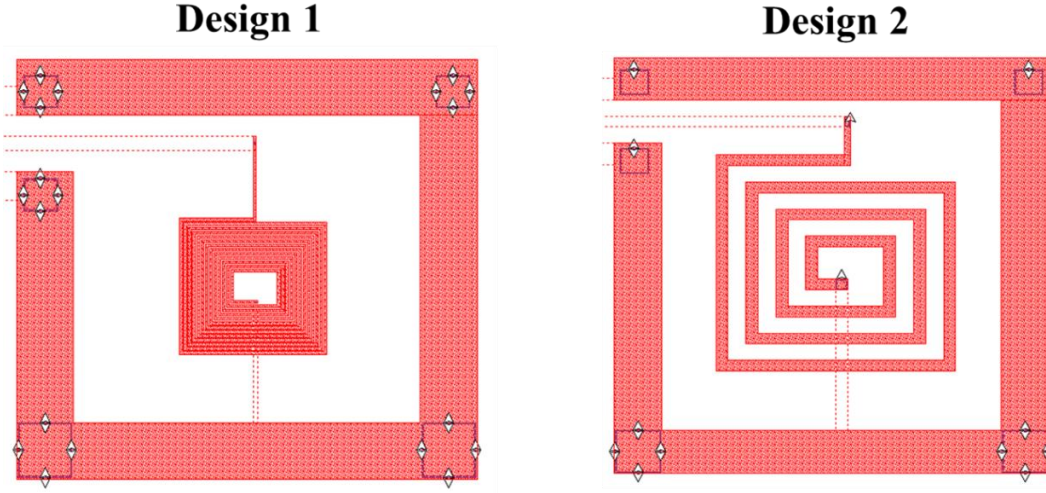


Fig. 5.1 - 3. Two Nb spiral with different physical dimensions.

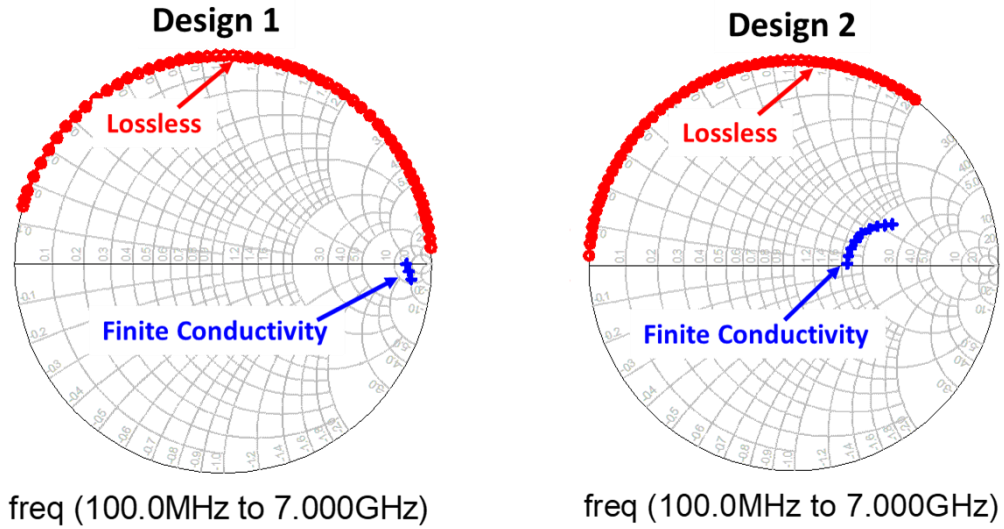


Fig. 5.1 - 4. EM simulation results of the two spiral structures in Fig. 5.1-3.

Figure 5.1-5 illustrates the 3D layout of the filter. The metal-insulator-metal capacitors and the spiral inductors are realized on layers M7 and M6 of the MIT-LL 8-Nb-layer fabrication process. Due to the nanometer thickness of the silicon dioxide layers and the multi-layer structure, the process allows for the realization of relatively very high capacitance and high inductance. With the DC current applied to the spiral inductor, the current density in the Nb metal traces can exceed the superconductor critical current level and the Nb metal traces of the spiral inductor switch from high conductivity to low conductivity. A Lakeshore Cryogenic Probe Station is used for the measurement.

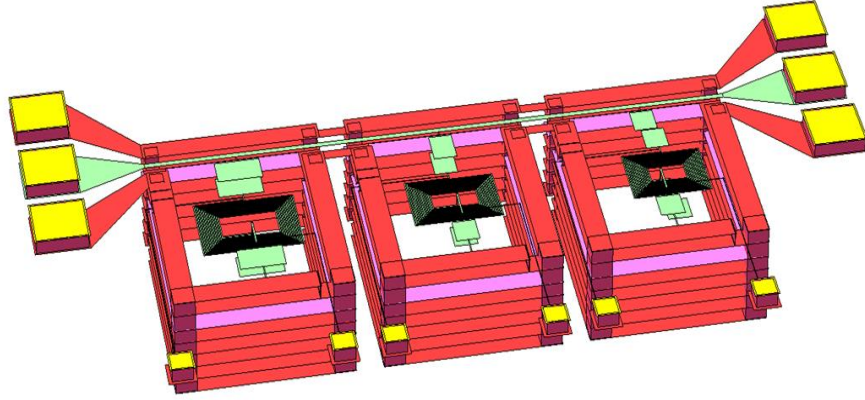


Fig. 5.1 - 5. The 3D layout of the proposed lumped-element Nb-based superconducting tunable band stop filter.

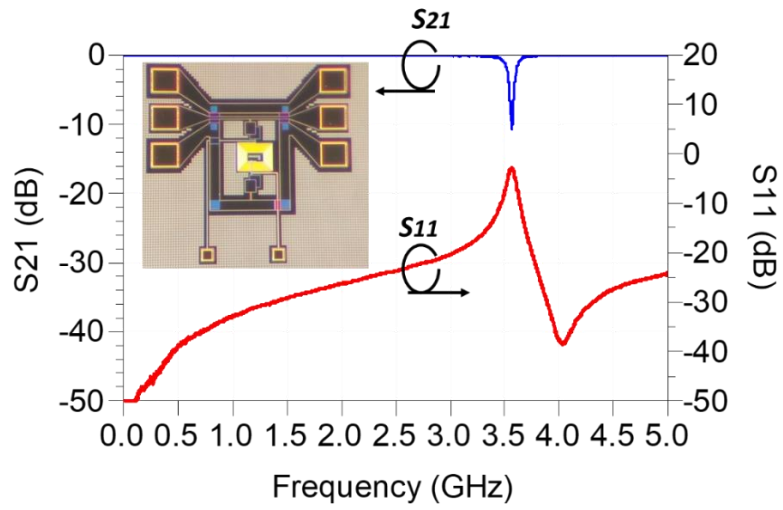


Fig. 5.1 - 6. The measurement results of a single band stop filter operates at the superconducting state.

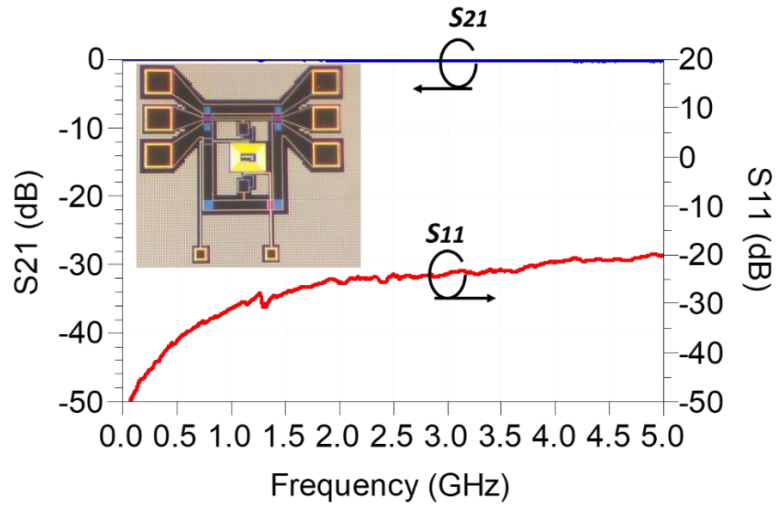


Fig. 5.1 - 7. The measurement results of a single band stop filter when DC current is applied to the Nb spiral inductor.

Figure 5.1-6 depicts the measurement results of a single band reject filter operating at the superconducting state. As one can see from Fig. 5.1-7, the band reject filter is turned off when the

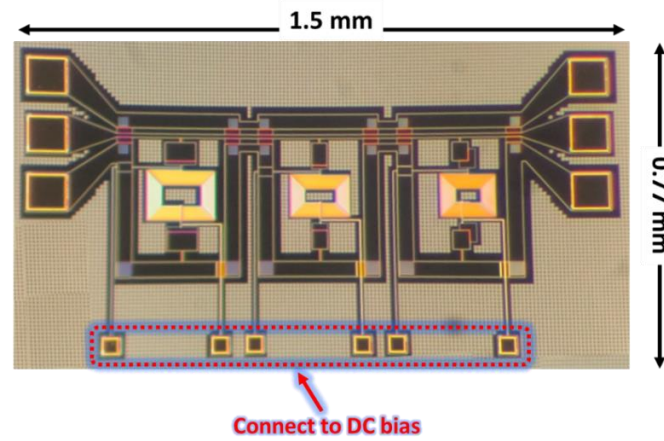


Fig. 5.1 - 8. Photo of the fabricated tunable band reject filter circuit.

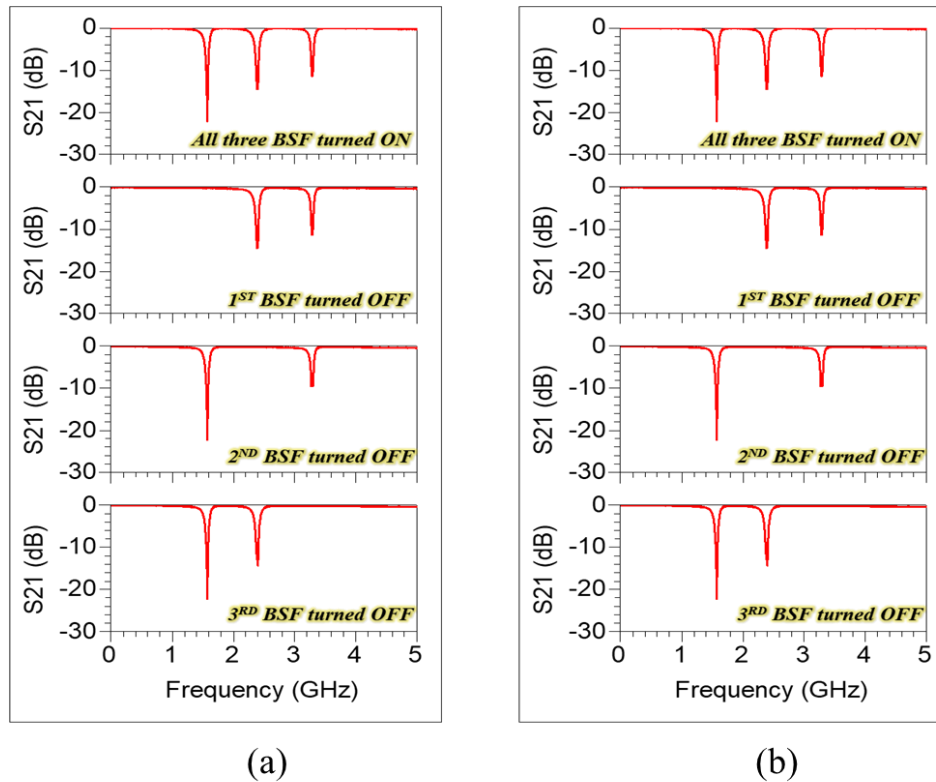


Fig. 5.1 - 9. (a) The measurement results when one rejection band is turned off. (b) The measurement results when two rejection bands are turned off simultaneously.

DC current is applied to the Nb spiral inductor. Figure 5.1-8 shows a photo of the band reject filter. Its size is 1.5 mm x 0.77 mm. Figure 5.1-9 (a) presents the measured results of the band reject filter when the DC current is applied only to one inductor, while Fig. 5.2-9 (b) depicts the measurement results when the DC current is applied to two inductors, i.e., two rejection bands are turned off simultaneously.

In this section, tunable band reject filters with a novel tuning mechanism are introduced using a unique feature of spiral inductors designed intentionally with high parasitic capacitance. It has been shown that such a spiral inductor performs as an inductor when its metal traces are made of high conductivity metals, while it performs as a capacitor when its metal traces are made of low conductivity. While the concept, is applied in this section to Nb superconductor spiral inductor, the same concept can be potentially employed to other type of materials whose conductivity can be switched from high value to low value through triggering by electrical, thermal, or optical means.

## 5.2 Nb-Based UWB Filter with Switchable Notches

Because of the ability of the superconductor ADC to digitize very wideband signals, the filters/multiplexers used in the front-end of the digital receivers are UWB filters. Such wideband on the other hand is susceptible to friendly/hostile interference from surrounding sources. The Nb-based tunable multiband reject filter introduced in the previous section can be used to develop a UWB bandpass filter with a switchable notch for interference cancelation. The two filters can be monolithically integrated together on a single chip, as shown in Fig. 5.2-1. This is a unique feature that superconductor electronics technology does not offer switches as the case with CMOS technology. The wideband coupler shown in Fig. 5.2-1 is needed to monitor the interference signal.

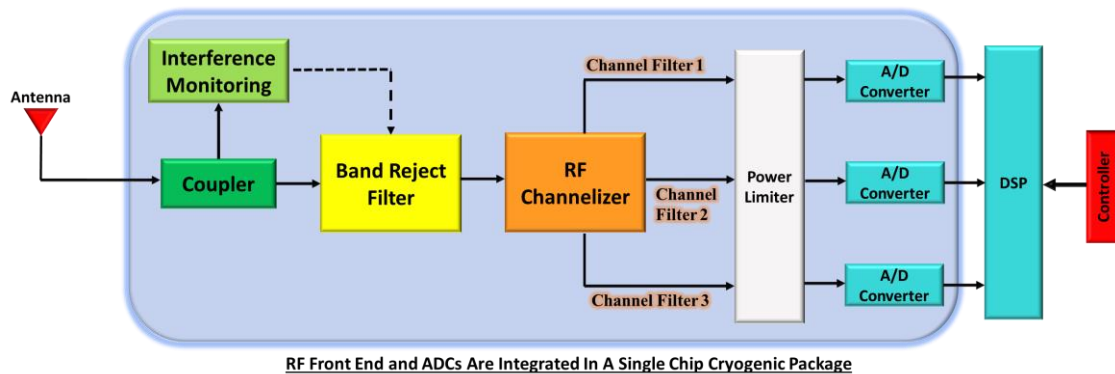


Fig. 5.2 - 1. The schematic block diagram of a superconductor RF front-end.

In addition to the ultra-wide superconductor  $\lambda g/4$  resonator filter demonstrated in Chapter 4, we present in this chapter an alternative design for the superconductor UWB filter. We also present theoretical and experimental results for ultra-wideband superconductor couplers.

Figure 5.2-2 shows the schematic of a stepped-impedance resonator (SIR). By carefully selecting the electrical length and impedance of each segment of the SIR, its first several resonant frequencies can be close to each other and thus form a multimode resonator (MMR). This type of SIR is widely employed to develop broadband filters [8] [64]. Figure 5.2-3 shows the schematic of the designed mm-Wave UWB triple-mode-resonator filter, which is developed using the MIT-LL 4-Nb-layer process.

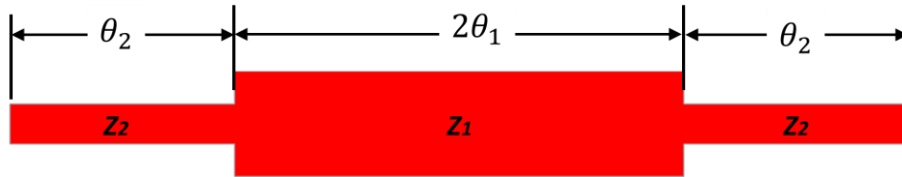


Fig. 5.2 - 2. The schematic of the stepped-impedance multimode resonator.

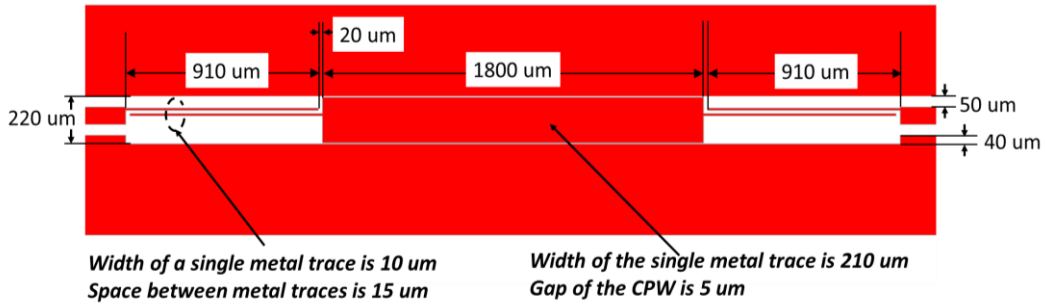


Fig. 5.2 - 3. The schematic of a mm-Wave UWB filter with one SIR MMR.

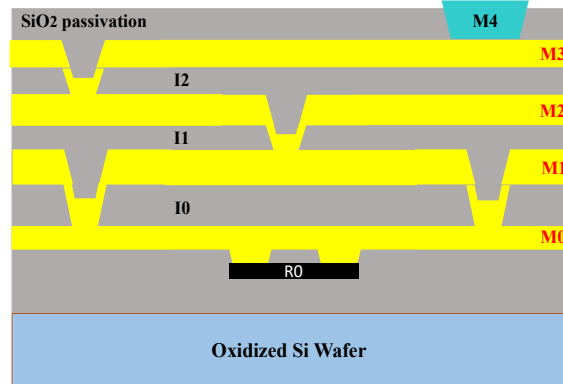


Fig. 5.2 - 4. The cross section of the MIT-LL 4-Nb-layer fabrication process. [49]

The MIT-LL 4-layer-Nb process, as depicted in Fig. 5.2-4, is a simplified version of the MIT-LL 8-layer-Nb process. Layers M0 - M3 are the Nb layers. The thickness of the Nb layer M0 is 150 nm, the thickness of Layer M1 is 250 nm, and the thicknesses of Layers M2 and M3 are both 200 nm. Moreover, Via I0 has a height of 500 nm, while Vias I1 and I2 have an identical height of 250 nm. The SiO<sub>2</sub> layer between Layer M0 and the oxidized Si wafer is 500 nm. A 250 nm thick gold layer M4 and a 40 nm thick lossy conductor layer R0 are also included in this process.

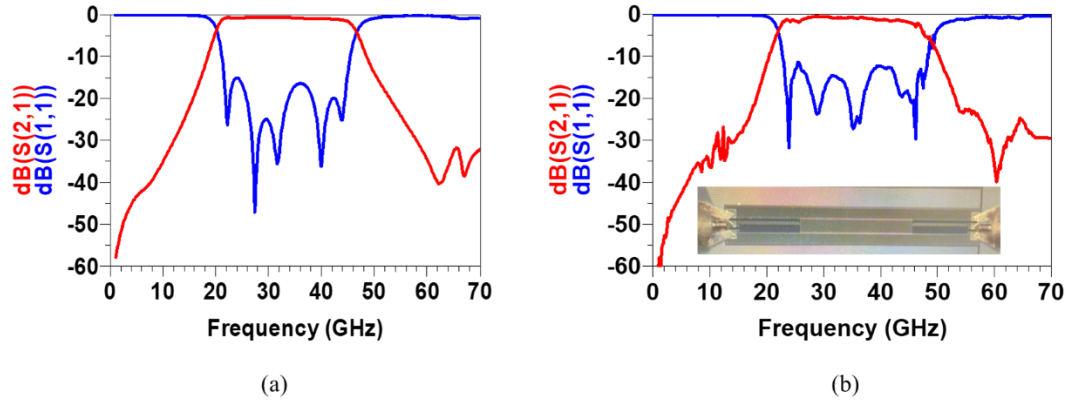


Fig. 5.2 - 5. (a) The EM-simulation result of the mm-Wave UWB triple-mode-resonator filter shown in Fig. 5.2-3. (b) The EM-simulation result of the mm-Wave UWB triple-mode-resonator filter shown in Fig. 5.2-3.

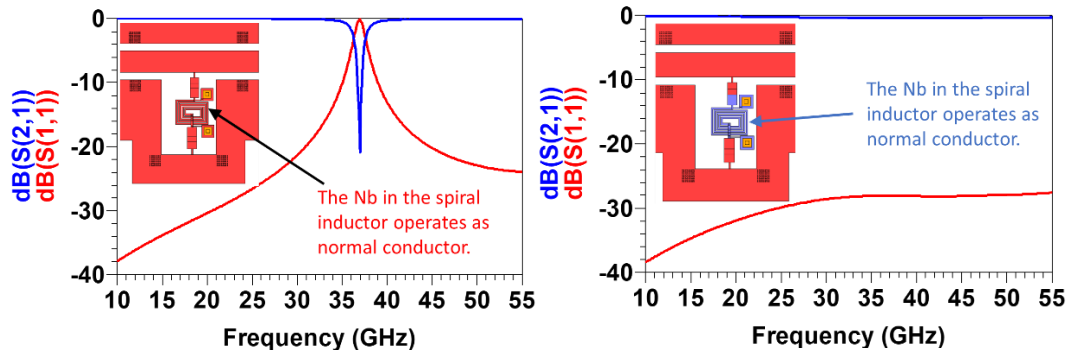


Fig. 5.2 - 6. The EM simulations results for the Nb in the spiral inductor operating in the superconducting state and the normal conductor state.

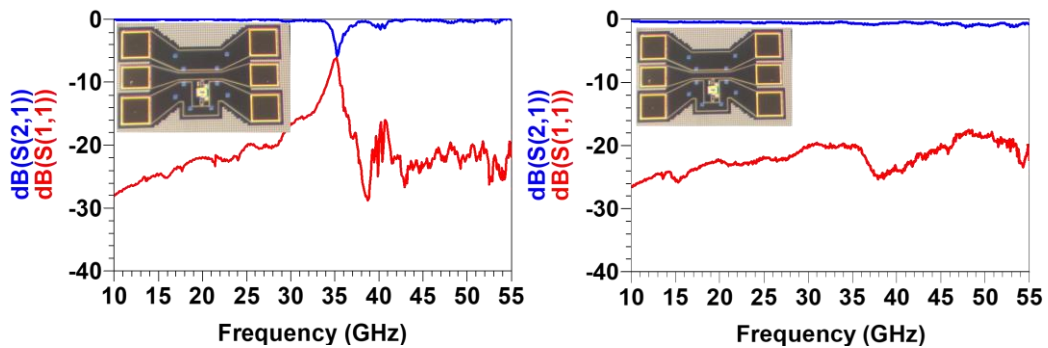


Fig. 5.2 - 7. The measurement results of the band reject filter with/without DC current applied to the spiral inductor.



The signal lines of the MMR UWB filter are built on the 1<sup>st</sup> Nb layer (M3) of the MIT-LL 4-Nb-layer process, and the ground plans are inserted to all the Nb layers connecting with vias. This ultra-wideband filter is designed with the center frequency of 33 GHz and a fractional bandwidth of 80%. The EM simulation and measurement results of this UWB filter are presented in Fig. 5.2-5.

The switchable band reject filter used in Fig. 5.2-1 is designed at 36 GHz with the same band reject filter architecture as was introduced in the previous section. Figure 5.2-6 shows the EM simulations results for the Nb in the spiral inductor operating in the superconducting state and normal conducting state, respectively. The measurement results are provided in Fig. 5.2-7.

After designing the band reject filter and the UWB bandpass filter, the Nb-based UWB bandpass filter with a switchable notch can be developed. The EM simulation and measurement results are given in Fig. 5.2-8 and Fig. 5.2-9, respectively. When the spiral inductor in the band reject filter operates in the superconducting state, a notch within the UWB filter's passband is created. When

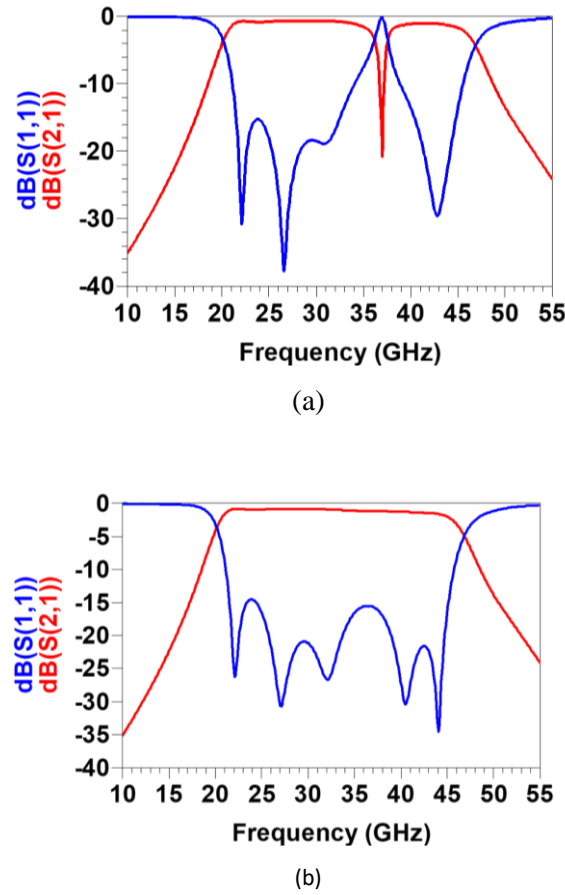
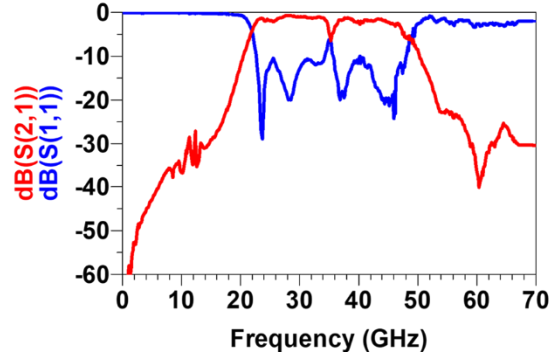
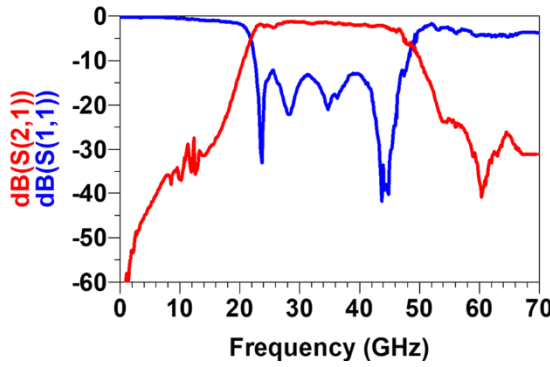


Fig. 5.2 - 8. The cascaded EM simulation results of the Nb-based mm-Wave MMR UWB bandpass filter with a switchable notch. (a). The spiral inductor in the band reject filter operates in the superconducting state. (b). The spiral inductor in the band reject filter operates in the normal conductor state.

the spiral inductor in the band reject filter operates in the normal conducting state, the band reject filter becomes a low-loss transmission line with no impact on the UWB filter's passband. This design can be extended to a UWB filter with multiple switchable notches.



(a)



(b)

Fig. 5.2 - 9. The cascaded measurement simulation results of the Nb-based mm-Wave MMR UWB bandpass filter with a switchable notch. (a). The spiral inductor in the band reject filter operates in the superconducting state. (b). The spiral inductor in the band reject filter operates in the normal conductor state.

## 5.3 Nb-based Superconductor Couplers

In superconductor digital receivers, ultra-wideband couplers with large coupling values are needed to monitor the presence of a high-power interference signal, while ultra-wideband 3dB couplers are needed in power limiter applications. Such power limiters are often needed for added protection to the superconductor ADC. To realize a UWB 3dB Lange coupler for mm-Wave applications, the fabrication process should be capable of realizing structures with fine feature size and crossovers. The MIT-LL multi-Nb-layer fabrication process is therefore optimum for realizing



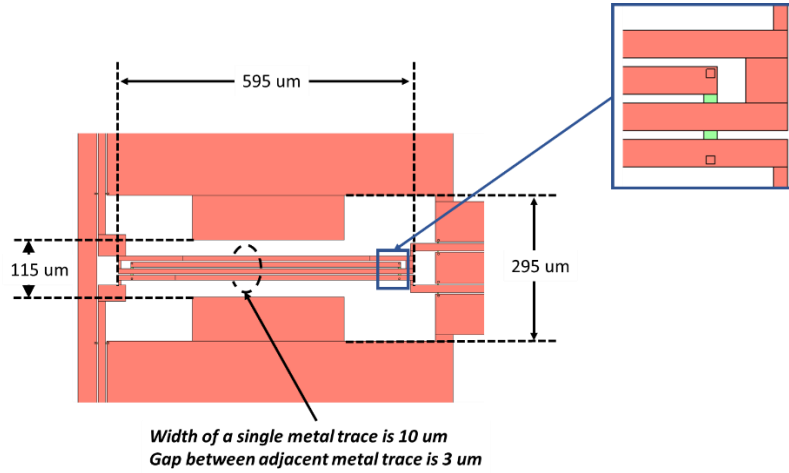


Fig. 5.3 - 1. The schematic of a designed Nb-based mm-Wave UWB 3 dB Lange coupler.

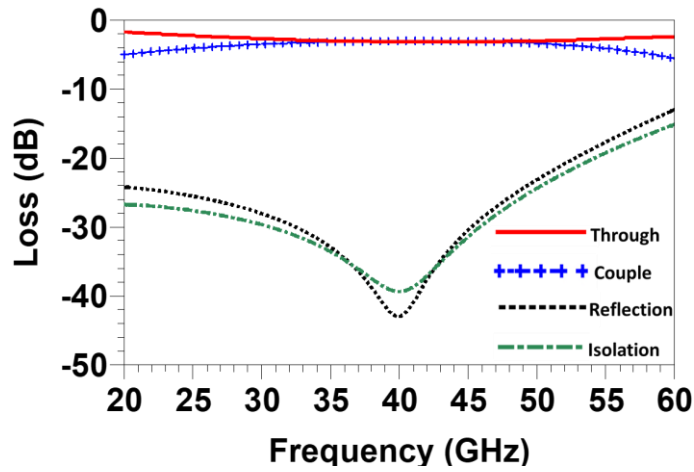


Fig. 5.3 - 2. The simulation results of the Nb-based mm-Wave UWB 3 dB Lange coupler.

such couplers. Figure 5.3-1 shows the schematic of a designed Nb-based mm-Wave UWB 3 dB Lange coupler using the MIT-LL 4-Nb-layer process. The signal lines are built on the 1<sup>st</sup> Nb layer (M3); the crossovers are built on the 2<sup>nd</sup> Nb layer (M2); and the ground plans are inserted into all the Nb layers connecting with vias. The EM simulation results are presented in Fig. 5.3-2. The MIT-LL 4-Nb-layer process also allows for the realizing of 50 Ohm loads by using the lossy conductor layer (R0). The design of the broadband 50 Ohm load is covered in section 4.3. As depicted in Fig. 5.3-3, two ports of the coupler are terminated to 50 Ohm loads when the other two ports are measured. Figure 5.3-4 shows the photos of the fabricated 3dB coupler couplers with 50 Ohm loads at different ports. The measurement results are provided in Fig. 5.3-5. As shown, the coupler exhibits a bandwidth of 25 GHz at a center frequency of 42 GHz, i.e., a fractional bandwidth close to 60%.

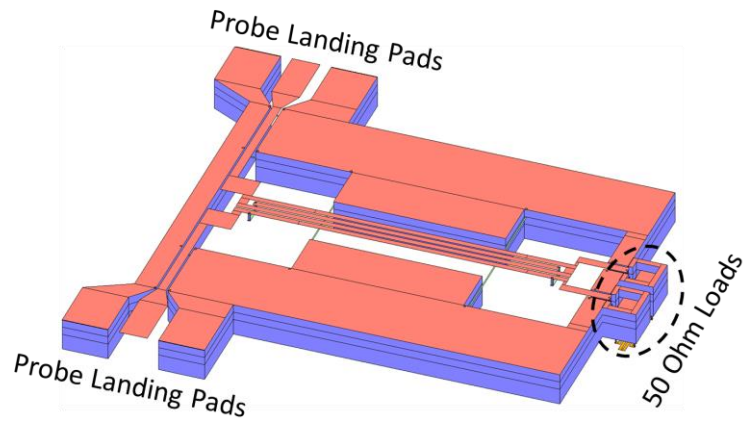


Fig. 5.3 - 3. The the 3D layout of the designed Nb-based mm-Wave UWB 3 dB Lange coupler.

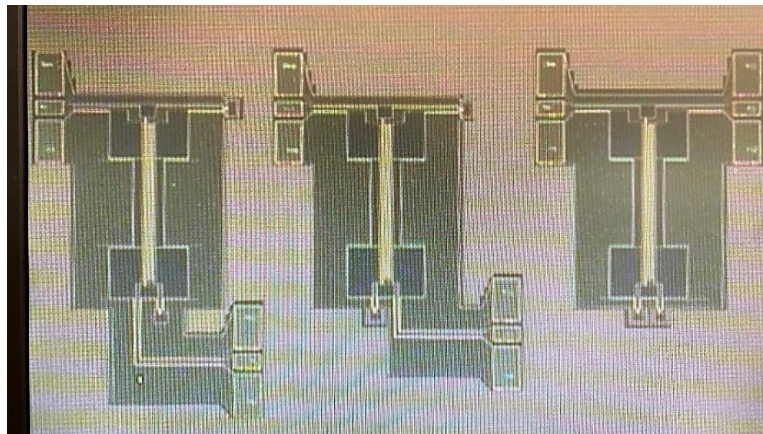


Fig. 5.3 - 4. The photos of the fabricated Lange couplers with 50 Ohm loads at different ports.

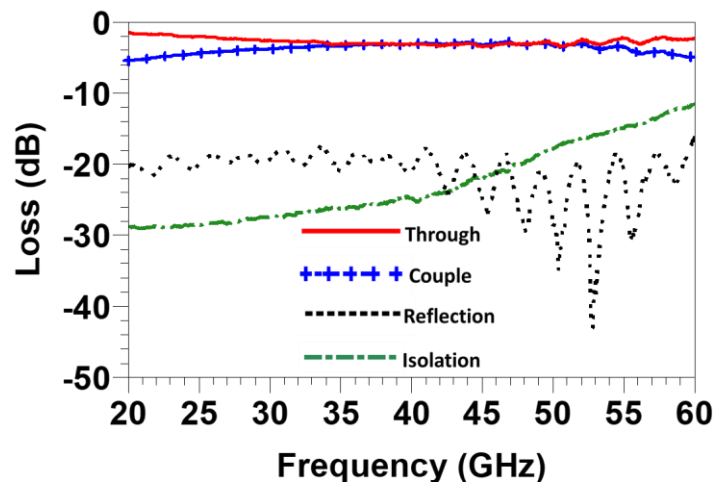


Fig. 5.3 - 5. The the measurement results of the designed Nb-based mm-Wave UWB 3 dB Lange coupler.

Figure 5.3-6 illustrates a 2D layout of an Nb-based 30 dB coupler. This layout is realized by cascading two 15 dB coupled line couplers. The single lines are shown in green and built on the 1<sup>st</sup> Nb layer (M7) of the MIT-LL 8-Nb-layer process. The ground planes are shown in red and built on all Nb layers. Figure 5.3-7 provides the EM simulation results. A photo of the fabricated couplers is shown in Fig. 5.3-8 and the measurement results are presented in Fig. 5.3-9. As can be seen, the coupler offers a coupling value of 30 dB over the frequency range of 25 - 65 GHz at a center frequency of 45 GHz, i.e., a fractional bandwidth close to 90%.

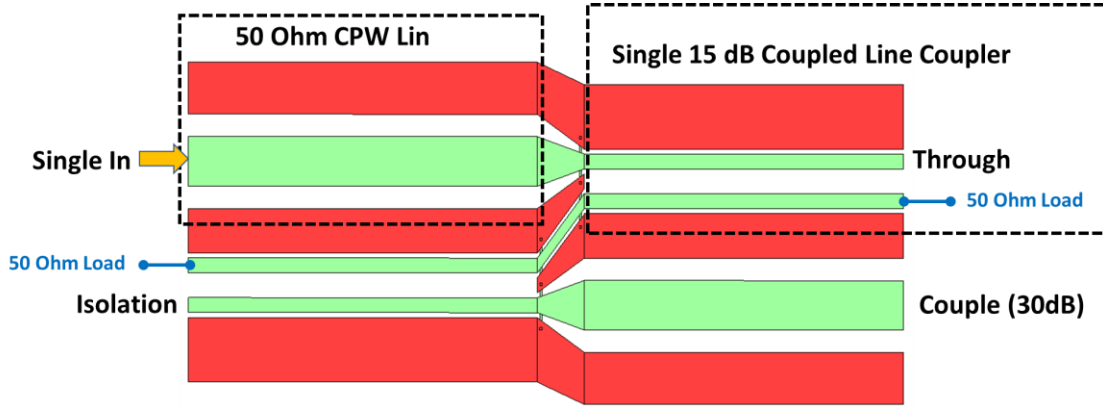


Fig. 5.3 - 6. The 2D layout of a Nb-based 30 dB coupler which is realized by cascading two 15 dB coupled line couplers.

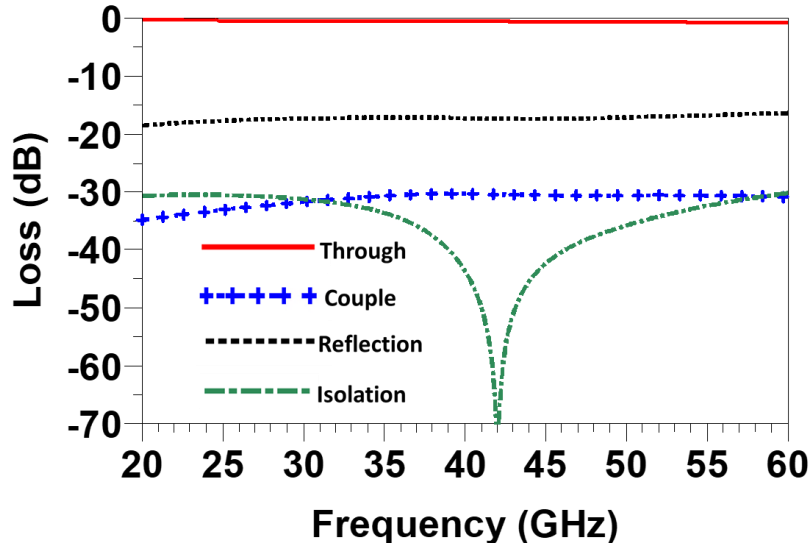


Fig. 5.3 - 7. The EM simulation results of the Nb-based 30 dB coupler.

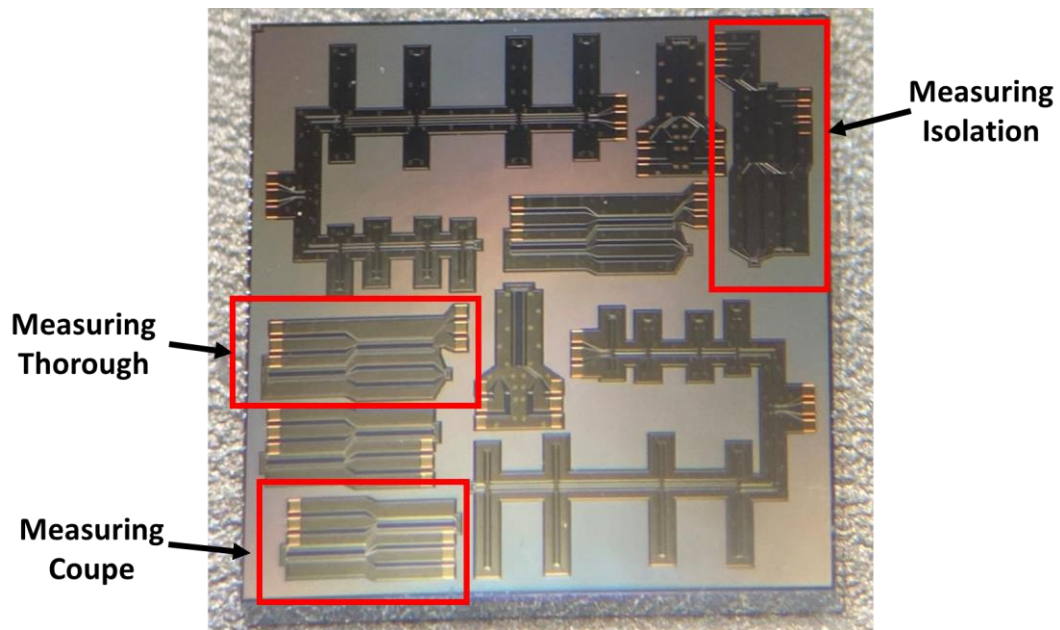


Fig. 5.3 - 8. The photo of the fabricated Nb-based 30 dB couplers with 50 Ohm loads at different ports.

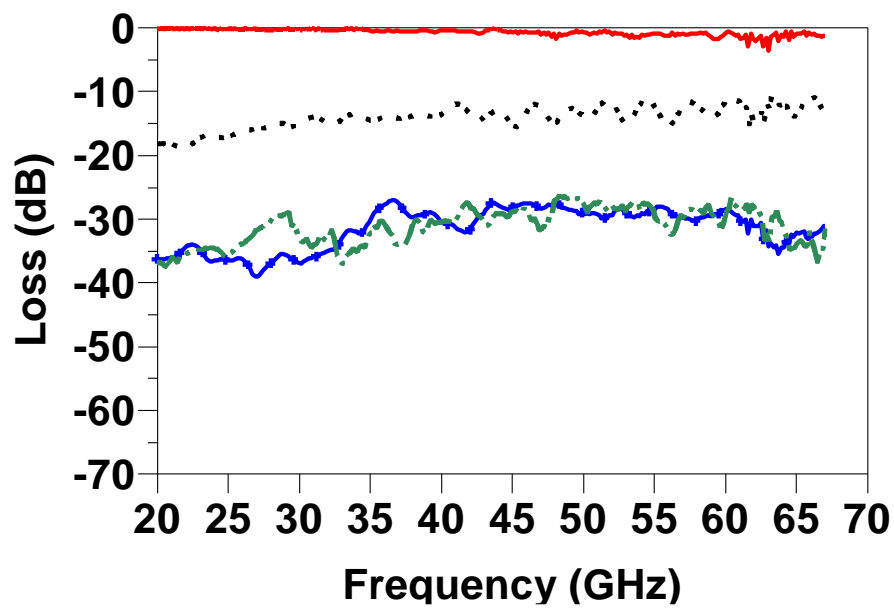


Fig. 5.3 - 9. The measurement results of the Nb-based 30 dB coupler.

# Chapter 6

## Mm-Wave Silicon-Micromachined Filters

Conventionally, to fabricate 3D resonators and filters, the designed structures are shaped on metal blocks by using computer numerical controlled (CNC) machining technologies or electrical discharge machining (EDM) technology. While EDM machining can be used to fabricate structures with fine feature sizes of around one hundred microns, the fabrication process is quite expensive and does not lend itself to mass production. The laser-cutting technology can be potentially used for surface micromachining. Because it is a thermal process, it is usually difficult to realize smooth surfaces with accurate dimensions. For example, Fig. 6.0-1 shows the photo of a structure fabricated using laser-cutting machining (done by a commercial company) and the Si-based DRIE micromachining process (done at the CIRFE lab at the University of Waterloo). As can be seen, the cutting edges of the stainless-steel pieces that were cut by laser machining are badly distorted, as a recast layer forms on the cutting edge due to the extreme high temperature of the laser beam.

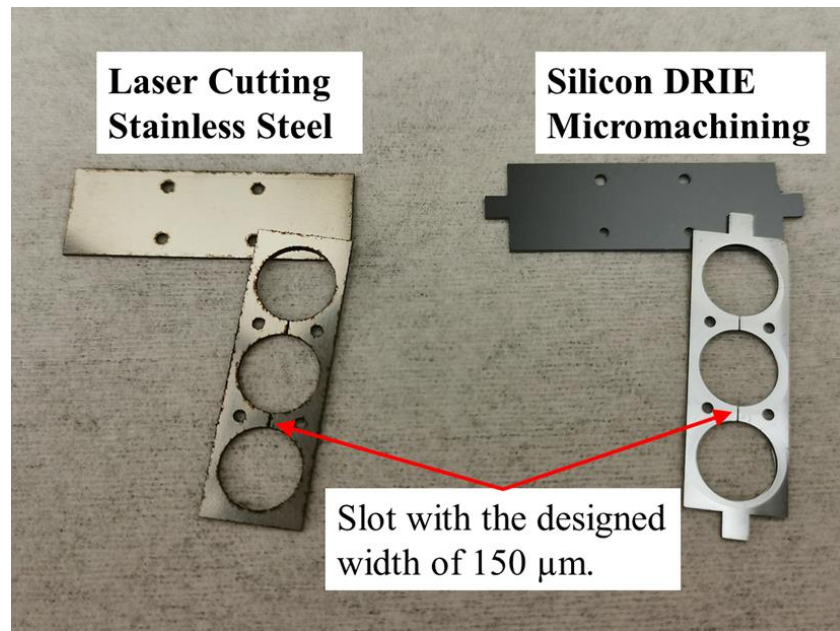


Fig. 6.0 - 1. The photo of a designed structure was fabricated by cutting the stainless steel with the CNC laser machine and by etching the Si wafer with the DRIE micromachining process.

Conventional machining of 3D resonators and filters for low-frequency applications has a bulky physical size, which allows to use tuning screws for post-fabrication tunings and compensating the manufacturing tolerance. As the operating frequencies increase to the mm-Wave frequency band, the physical size of the 3D resonator becomes compact. When this occurs, it is impossible to compensate the manufacturing tolerance by use of tuning screws. Silicon-micromachining technologies use short wavelength lights (e.g., Ultraviolet light, X-ray, e-beams) to transfer the designed geometric patterns to a thin light-sensitive photoresist layer on the substrate. Subsequent processing steps are then used to build patterns on the substrate with chemical- and molecular-level physical treatments, as explained in section 2.4. Therefore, silicon-micromachining fabrication processes provide much higher manufacturing accuracy than traditional machining technologies.

As reviewed in Chapter 2, the Si-DRIE process has been widely used to develop waveguide filters for mm-Wave and THz applications with extraordinary manufacturing accuracy [23]-[25]. Currently, most of the reported Si-DRIE micromachining filters use simple waveguide resonators. Section 6.1 presents filter designs composed of miniature ridge waveguide resonators. The proposed filter design provides highly compact physical size with reasonable high- $Q$  values, and can easily be fabricated with Si-DRIE technology. In Section 6.2, an ultra-high- $Q$  cavity filter is designed using the  $TE_{01}$  mode of a cylinder cavity resonator. In order to develop an ultra-high- $Q$  cavity filter using the  $TE_{01}$  mode of the cylindrical cavity resonator, it is necessary to separate the  $TM_{11}$  mode, since the two modes  $TE_{01}$  and  $TM_{11}$  are degenerate. The most efficient technique for separating the  $TM_{11}$  mode from the  $TE_{01}$  mode is forming the cylinder cavity into a barrel-shape [65]-[66]. However, the barrel-shape cavity proposed in [65] cannot be fabricated by the Si-DRIE process. In section 6.2, the barrel-shape cavity resonator is redesigned so that it can be fabricated with the DRIE process.

## 6.1 Miniature Ridge Waveguide Resonator Filters

Waveguide resonators have been widely used for low-loss RF applications due to their high- $Q$  values. However, their bulky physical sizes limit their use in miniaturized applications. To reduce the physical size of the waveguide resonator, several techniques have been developed.

One approach to reduce the physical size of the waveguide resonator is to load it with high dielectric constant material to fill the metallic cavity. As shown in Fig. 6.1-1, the air-filled gold cavity resonator has the physical size of 8.3 mm x 8.3 mm x 1 mm at the resonant frequency of 25.5 GHz, with a  $Q$  value of 1,640. In contrast, the alumina substrate-filled gold cavity resonator has a more compact physical size of 2.72 mm x 2.72 mm x 1 mm at the same resonant frequency



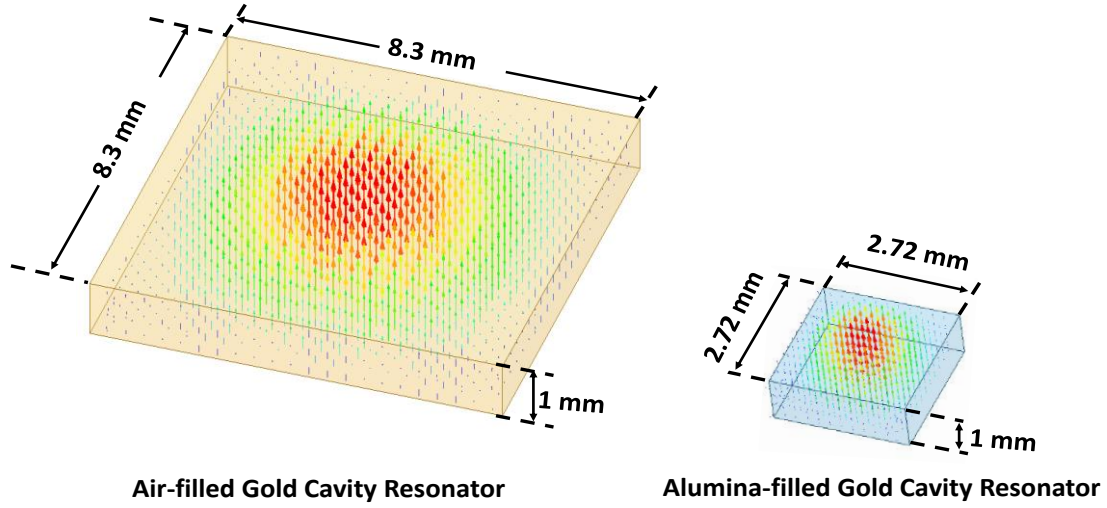


Fig. 6.1- 1. The dimensions of an air-filled gold cavity resonator and an alumina-filled gold cavity resonator with the 1<sup>st</sup> resonant mode at 25.5 GHz.

of 25.5 GHz at expense of a lower  $Q$  value of 740. This type of dielectric-filled cavity resonator is referred as the monoblock dielectric resonator filter. To fabricate the monoblock dielectric resonator filter, the dielectric planks can be machined to designed shapes by using laser cutting machines or waterjet cutting machines, after which the machined dielectric planks are coated with metals. Several monoblock dielectric resonator filters have been reported in the literature [67]-[69].

Another solution for reducing physical size is using ridge waveguide resonators [70]-[71]. Figure 6.1-2 shows the dimensions of a ridge waveguide resonator designed at the resonant frequency of 25.5 GHz. As can be seen, this resonator has a much smaller footprint than the resonators shown in Fig. 6.1-1. Ridge waveguide resonators can be fabricated on Si wafers by using DRIE technology. However, in order to get a reasonable  $Q$ , the thickness of the Si wafer needs to be greater than 1 millimeter to fabricate the ridge waveguide resonator shown in Fig. 6.1-2, yet the thickness of standard Si wafers is only a few hundred micrometers. In addition, using thick silicon wafers complicates the DRIE process. Alternatively, we propose the dielectric loaded double-ridge waveguide resonator shown in Fig. 6.1.3. This resonator consists of three parts. The top and bottom parts (shown in gold color) can be fabricated by applying Si-DRIE on standard Si wafers (a standard 4-inch Si wafer is 525  $\mu\text{m}$  thick). A 254- $\mu\text{m}$  thick alumina wafer is then sandwiched between the two processed Si wafers, as shown in Fig. 6.1-3. The  $Q$  value of this resonator at 25.5 GHz is 470.

Figure 6.1-4 highlights a comparison between the air-filled metallic cavity resonator shown in Fig. 6.1-1 and the dielectric loaded double-ridge waveguide resonator depicted in Fig. 6.1-3. As one can see, the physical volume of the dielectric loaded double-ridge waveguide resonator is 3%

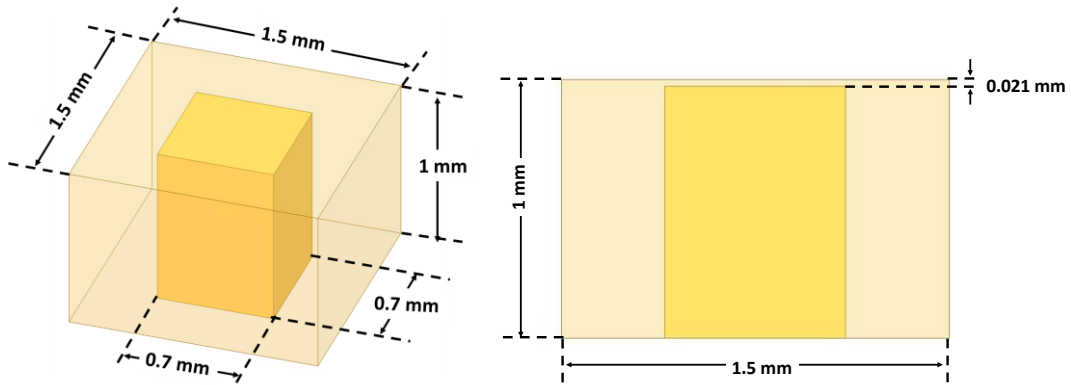


Fig. 6.1- 2. The dimensions of a single ridge waveguide resonator with the 1<sup>st</sup> resonant mode at 25.5 GHz.

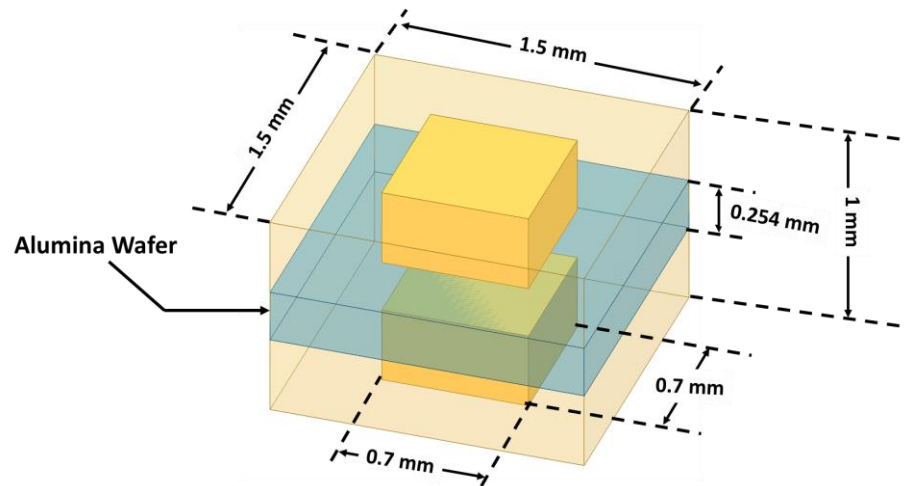


Fig. 6.1- 3. The dimensions of a dielectric loaded double-ridge waveguide resonator with the 1<sup>st</sup> resonant mode at 25.5 GHz.

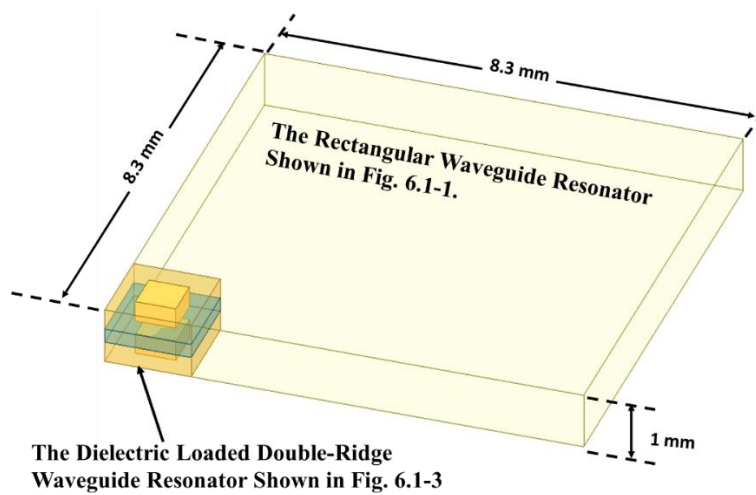


Fig. 6.1- 4. Comparing the dimensions of an air-filled gold cavity resonator with a dielectric loaded double-ridge waveguide resonator. The 1<sup>st</sup> modes of both resonators are at 25.5 GHz.



the volume of the air-filled waveguide resonator. The dielectric loaded double-ridge waveguide resonator is roughly 30% the volume of the monoblock dielectric loaded waveguide resonator shown in Fig. 6.1-1, Moreover, it is amenable to mass production through Si-DRIE processes.

The physical size of the dielectric loaded double-ridge waveguide resonator illustrated in Fig. 6.1-3 can be further reduced by replacing the ridges with the T-septum shapes presented in Fig. 6.1-5 (this resonator has a resonant frequency of 20 GHz). The variation of the ridge waveguide resonator is referred to as the T-septum resonator and was first proposed in [72]-[74]. The properties of the T-septum resonator are discussed in [75] and [76].

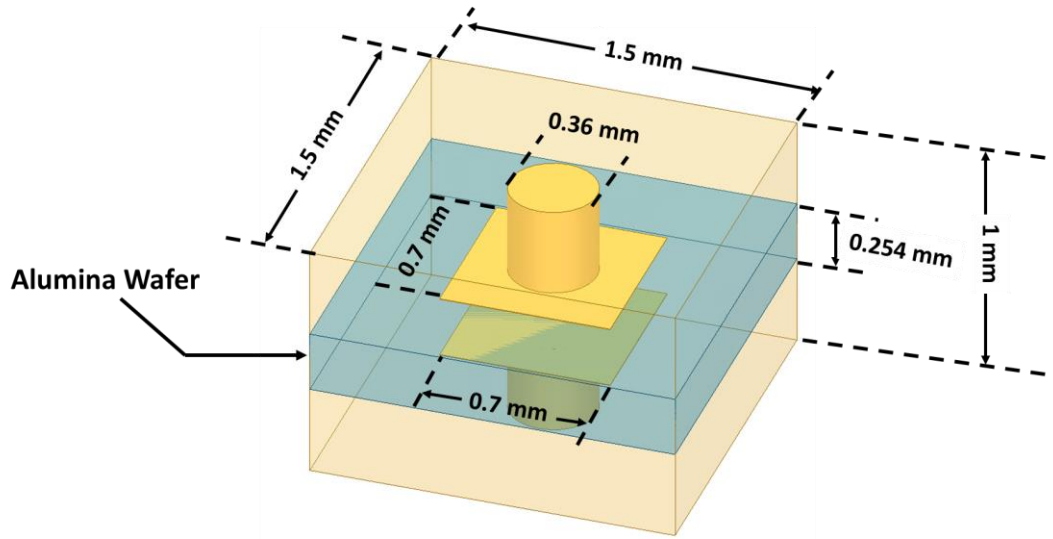


Fig. 6.1- 5. The dimensions of a dielectric loaded double-T-Septum waveguide resonator with the 1<sup>st</sup> resonant mode at 20 GHz.

Figure 6.1-6 shows the 3D layout of a 4-pole dielectric loaded double-T-septum resonator bandpass filters operating at the center frequency of 25.5 GHz with a fractional bandwidth of 11.7%. This filter has a compact physical size of 4.7 mm x 4.7 mm x 1.3 mm. The top and bottom parts of the filter are fabricated on a standard 4-inch Si wafer by using DRIE, and a 3  $\mu$ m thick gold layer is coated on the processed Si wafer. The middle part of the filter is fabricated on a 254  $\mu$ m thick alumina substrate. The 50 Ohm CPW lines are used as the input and output ports of this filter. The simulated performance of this filter is presented in Fig. 6.1-7, while its dimensions are given in Fig. 6.1-8 to Fig. 6.1-10.

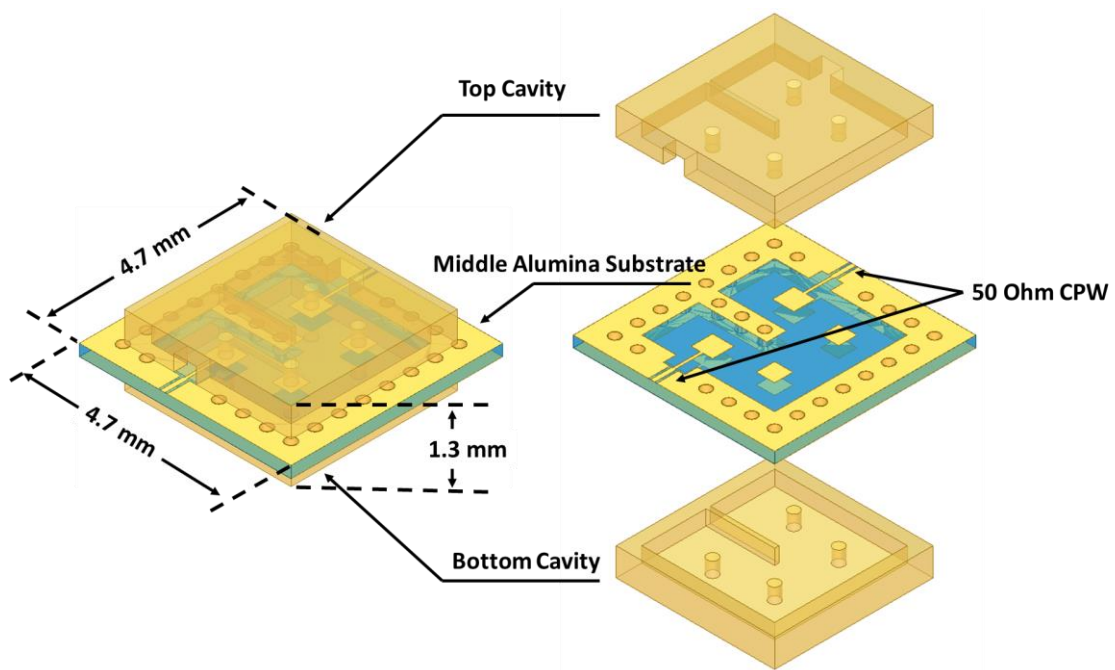


Fig. 6.1- 6. The 3D view and the layer-by-layer view of an mm-Wave dielectric loaded double-T-Septum waveguide resonator filter.

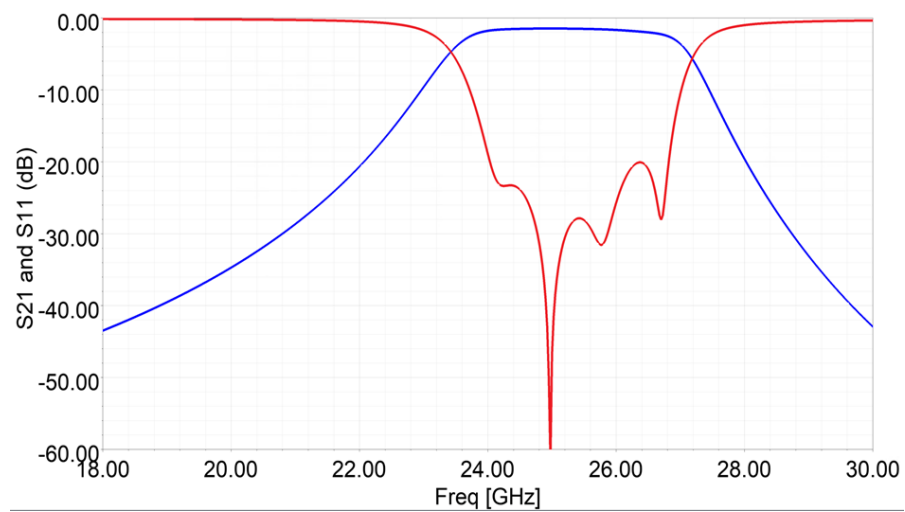


Fig. 6.1- 7. The simulation results of the mm-Wave dielectric loaded double-T-Septum waveguide resonator filter.

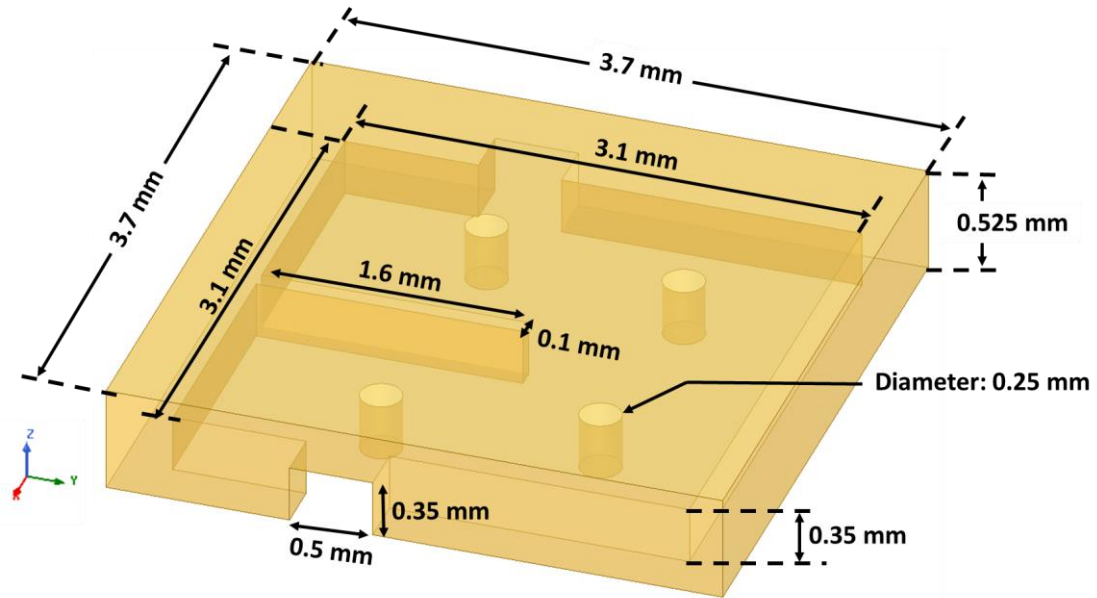


Fig. 6.1- 8. The dimensions of the top part of the mm-Wave dielectric loaded double-T-Septum waveguide resonator filter.

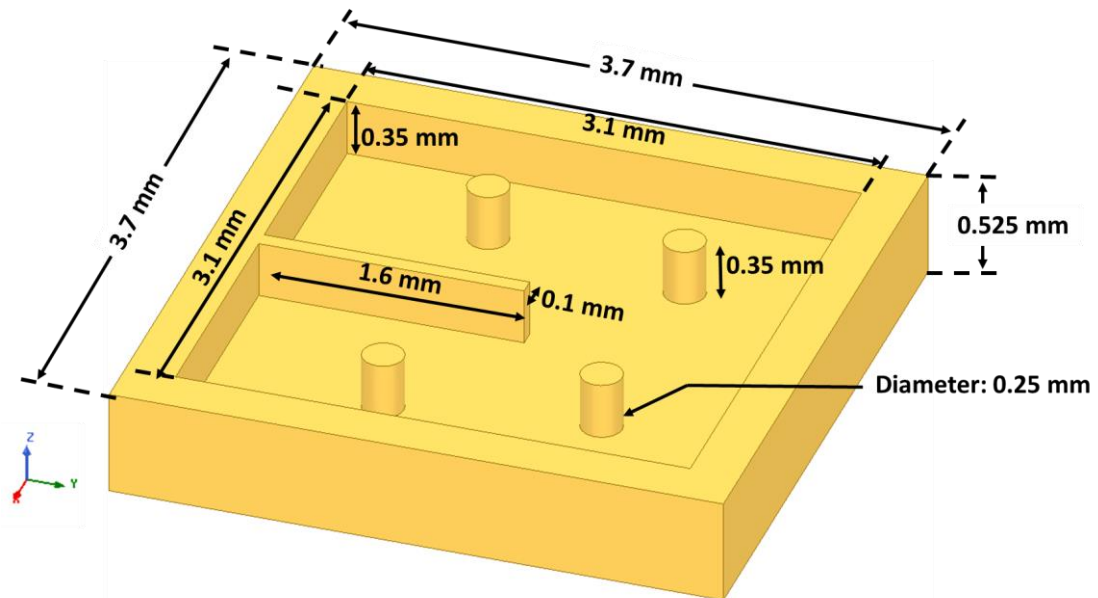


Fig. 6.1- 9. The dimensions of the bottom part of the mm-Wave dielectric loaded double-T-Septum waveguide resonator filter.



Figure 6.1-11 shows the 3D layout of another 4-pole dielectric loaded double-T-septum resonator bandpass filter designed at the center frequency of 7.425 GHz and with a fractional bandwidth of 47% (as shown in Fig. 6.1-12). This wideband filter requires strong couplings between the adjacent resonators. The strong inter-resonator couplings can be achieved by using conductor traces that bridge adjacent resonators. This filter is also designed with 50 Ohm CPW lines as the input and output ports. The dimensions of the filter are provided in Fig. 6.1-13 – Fig. 6.1-15.

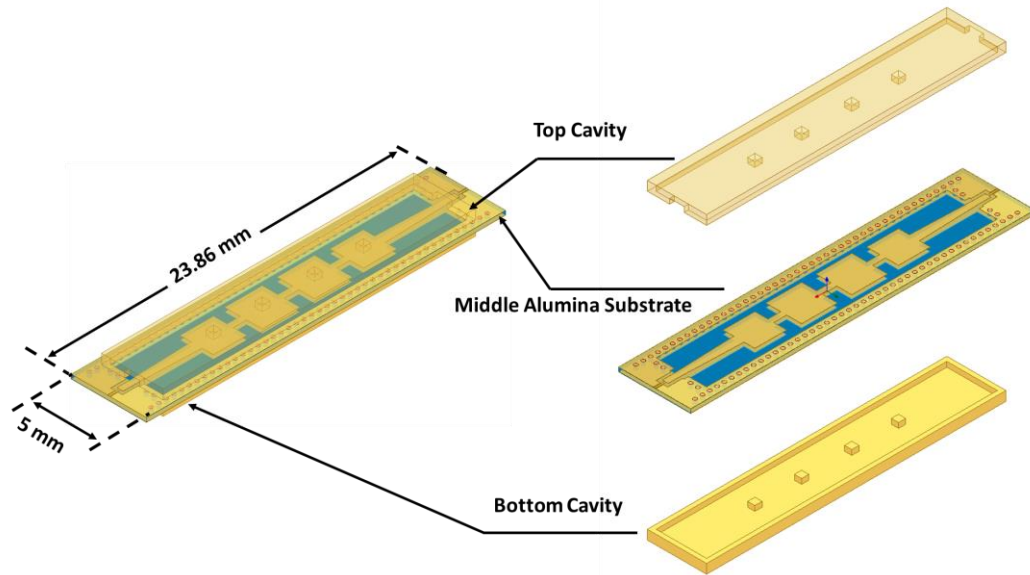


Fig. 6.1- 11. The 3D view and the layer-by-layer view of a wideband dielectric loaded double-T-Septum waveguide resonator filter.

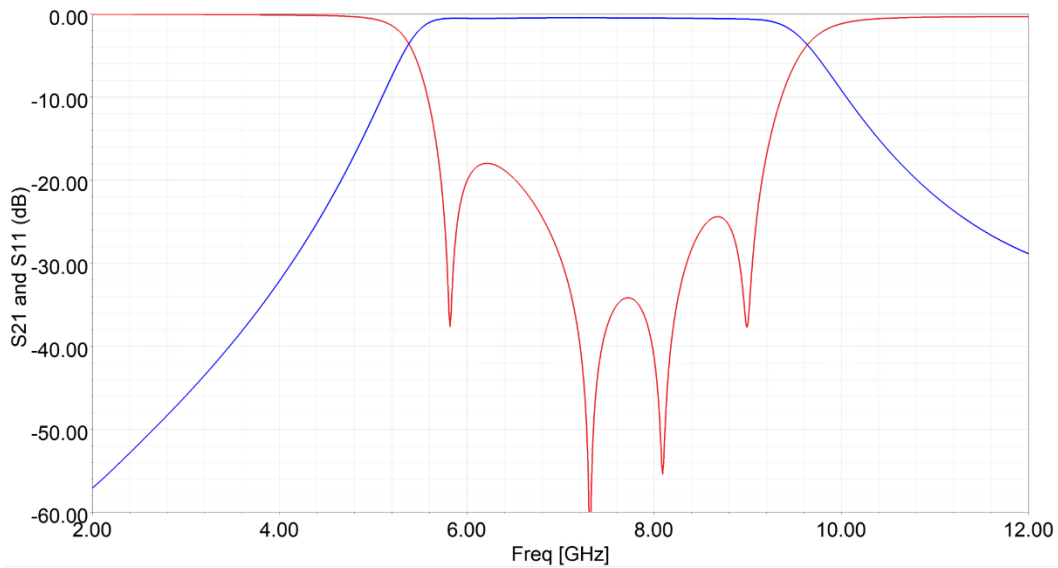


Fig. 6.1- 12. The simulation results of the wideband dielectric loaded double-T-Septum waveguide resonator filter.

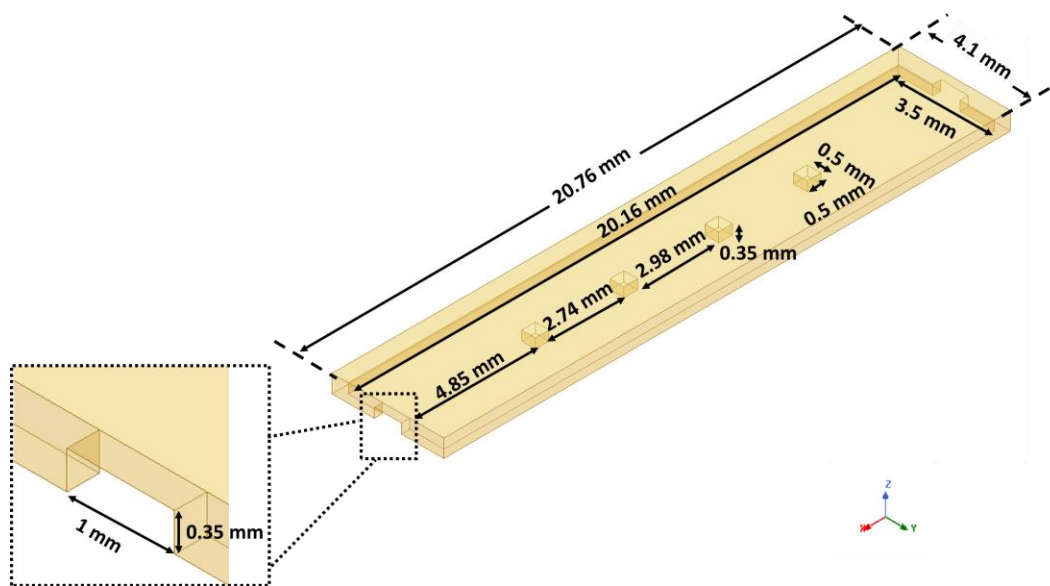


Fig. 6.1- 13. The dimensions of the top part of the wideband dielectric loaded double-T-Septum waveguide resonator filter.

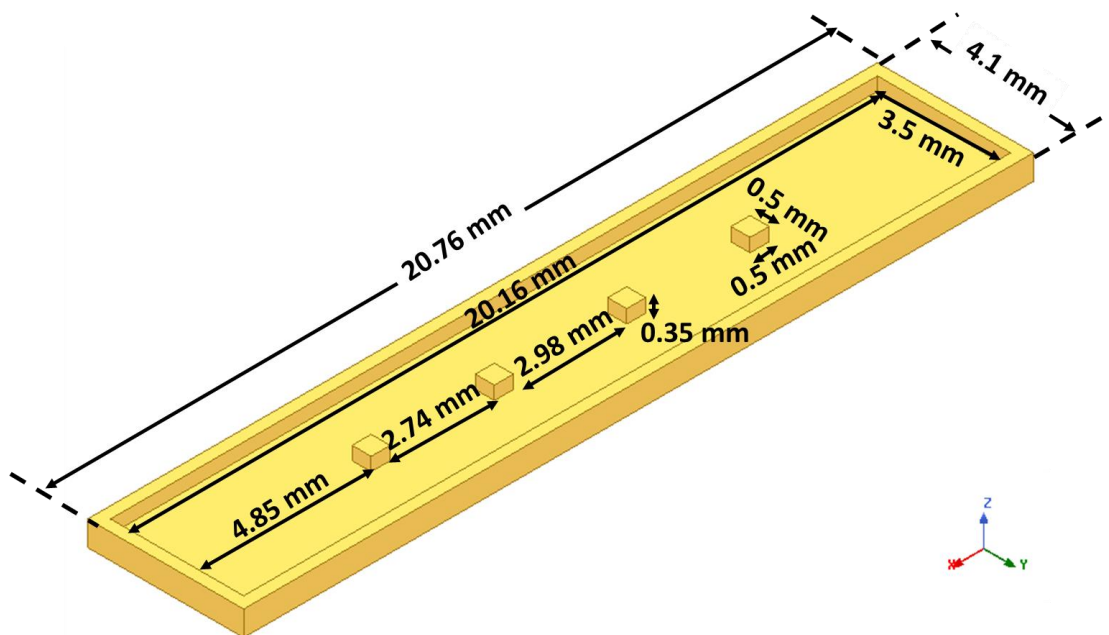


Fig. 6.1- 14. The dimensions of the bottom part of the wideband dielectric loaded double-T-Septum waveguide resonator filter.



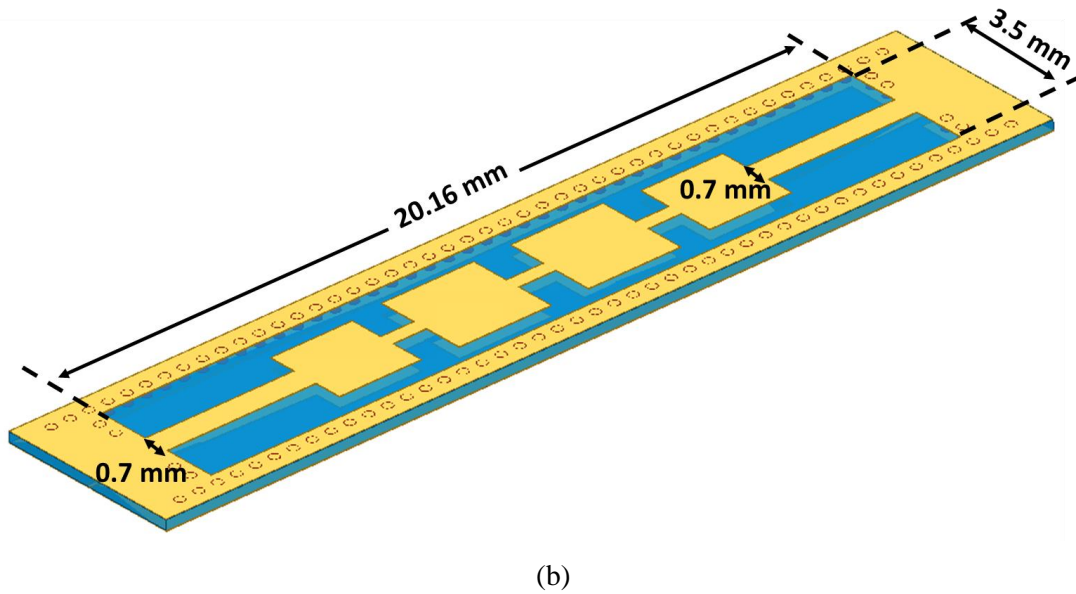
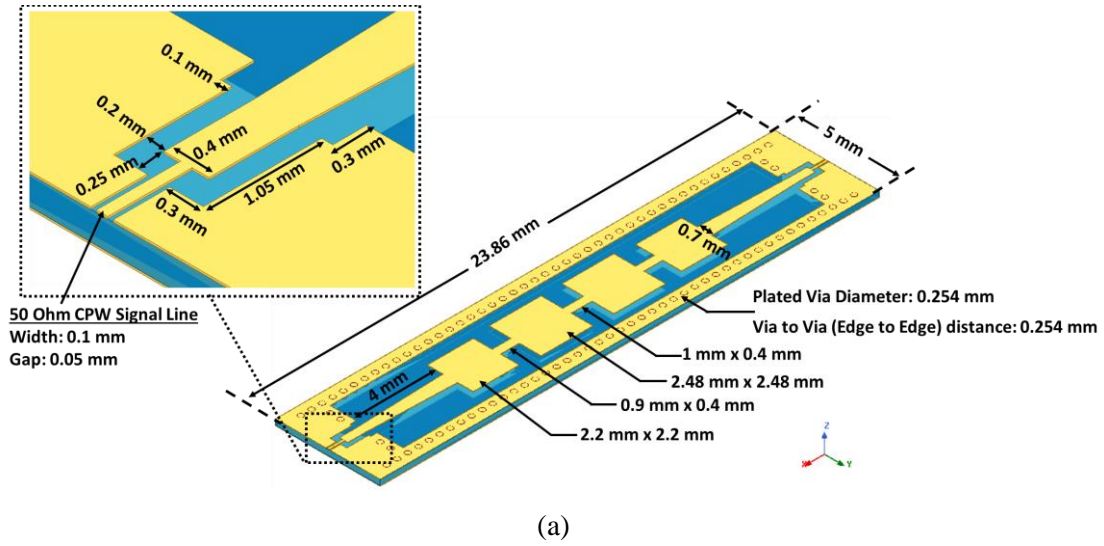


Fig. 6.1- 15. The dimensions of the bottom part of the wideband dielectric loaded double-T-Septum waveguide resonator filter.

Figure 6.1-16 shows a 4-pole quasi-elliptic filter with two transmission zeros at both sides of its passband. The two transmission zeros are generated by introducing a negative coupling between the first and last resonators. This filter is designed at the center frequency of 3.8 GHz and with a fractional bandwidth of 10%. The 375  $\mu\text{m}$  thick middle dielectric substrate has a dielectric constant of 30 and a loss tangent of  $6.7 \times 10^{-5}$  measured at 10 GHz. Nowadays, substrates with a high dielectric constant, low loss, and a thickness from 254  $\mu\text{m}$  to 10 mm are commercially available [77]. The simulation results of this highly miniature filter show that the minimum insertion loss

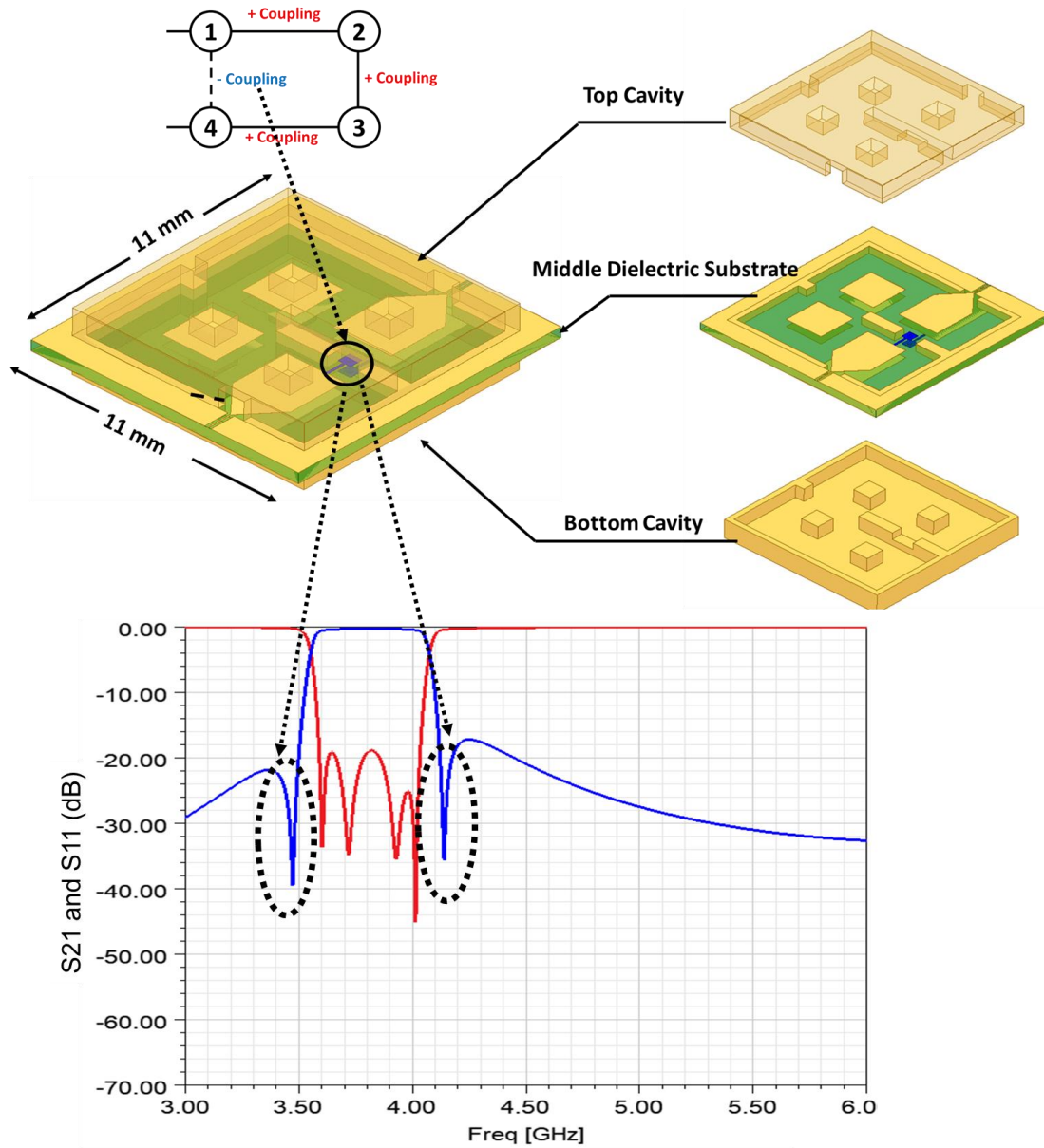


Fig. 6.1- 16. The 3D view, the layer-by-layer view and the simulation results of a Sub-6GHz dielectric loaded double-T-Septum waveguide resonator filter.

within the passband is 0.34 dB, which makes it useful for 5G sub-6-GHz miniature, low-cost, wideband applications.

Figure 6.1-17 and Fig. 6.1-18 plot the electric field distributions of the low and high modes for both the positive and negative coupling structures used in the filter shown in Fig. 6.1-16. For the positive coupling structure, the low mode electric fields of the two resonators have the same direction, while the high mode electric fields have opposite directions. In contrast, for the negative



coupling structure illustrated in Fig. 6.1-18, the low mode electric fields of the two resonators have the opposite directions, while the high mode electric fields have the same direction.

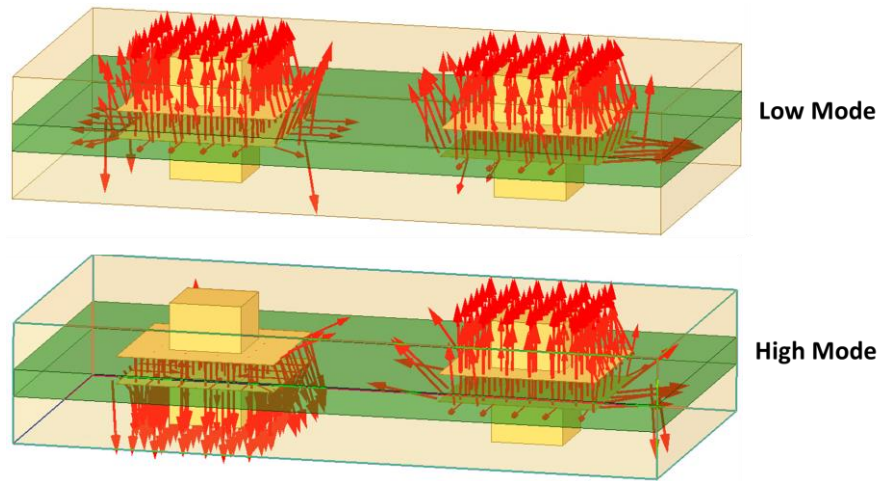


Fig. 6.1- 17. The electric field distributions of the low and high modes for the positive coupling structure used in the Sub-6GHz dielectric loaded double-T-Septum waveguide resonator filter.

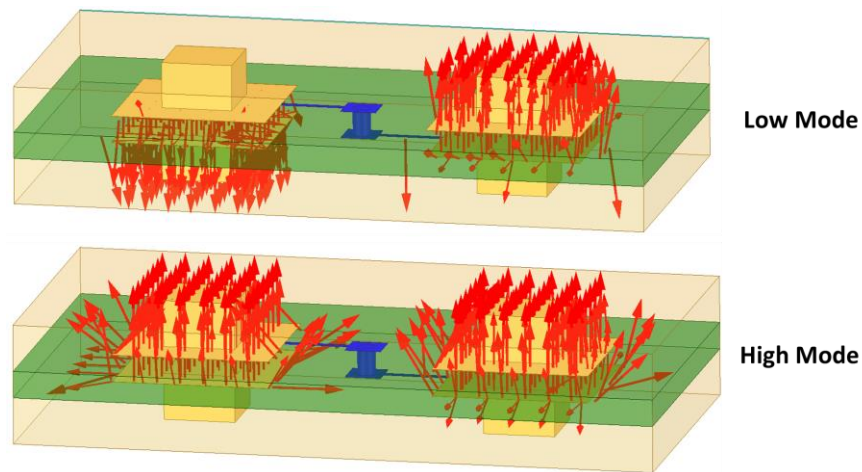


Fig. 6.1- 18. The electric field distributions of the low and high modes for the negative coupling structure used in the Sub-6GHz dielectric loaded double-T-Septum waveguide resonator filter.

## 6.2 Ultra-High- $Q$ Cylindrical Cavity Resonator Filter

While propagating in the atmosphere, mm-Waves can suffer severe attenuation from a variety of sources. Especially, as shown in Fig. 6.2-1, mm-Waves have an attenuation peak at 60 GHz while propagating in the atmosphere due to the presence of oxygen. Therefore, the 60 GHz mm-Wave not suitable for radar and long distances wireless communications. Nevertheless, the 60 GHz mm-

Wave can be used to provide communication with massive data rate between satellites, since there is almost no oxygen in high Earth orbit [1]; it can also be used for communication terminals that are within viewing range (i.e., not far from each other). Several ultra-high- $Q$  filters have been reported using the higher resonant modes of the cylindrical cavity resonators [66] [79] - [82]

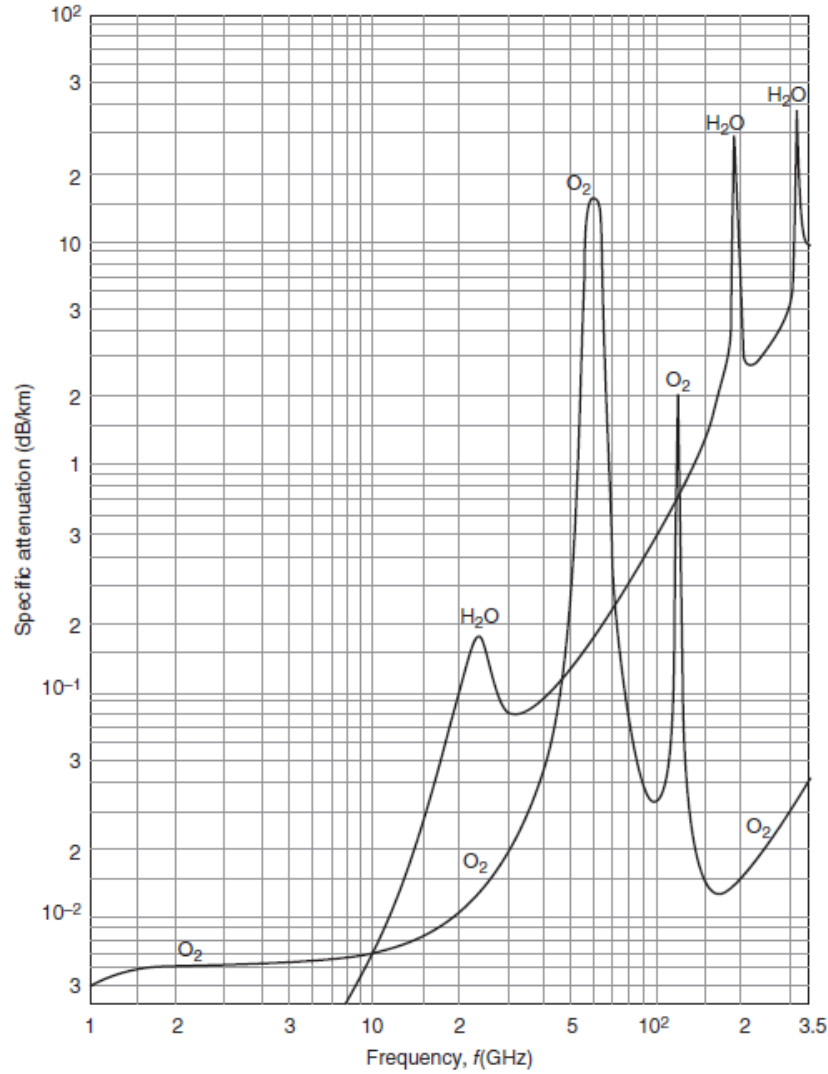


Fig. 6.2 - 1. Atmospheric losses as a function of frequency. [78]

The  $TE_{011}$  mode of cylindrical cavity resonator is very attractive for developing high- $Q$  filters. It is well-known that the  $TE_{011}$  mode has a significantly higher  $Q$  than the lower-order  $TE_{111}$ ,  $TM_{010}$  and  $TM_{111}$  modes. Unfortunately, the  $TE_{011}$  mode of operation degenerates with a pair of low- $Q$   $TM_{111}$  modes, as shown in Fig. 6.2-2. Therefore, the first challenge in developing a high- $Q$  cylindrical cavity resonator filter using the  $TE_{011}$  mode is to separate the  $TM_{111}$  mode from the  $TE_{011}$  mode. [83]

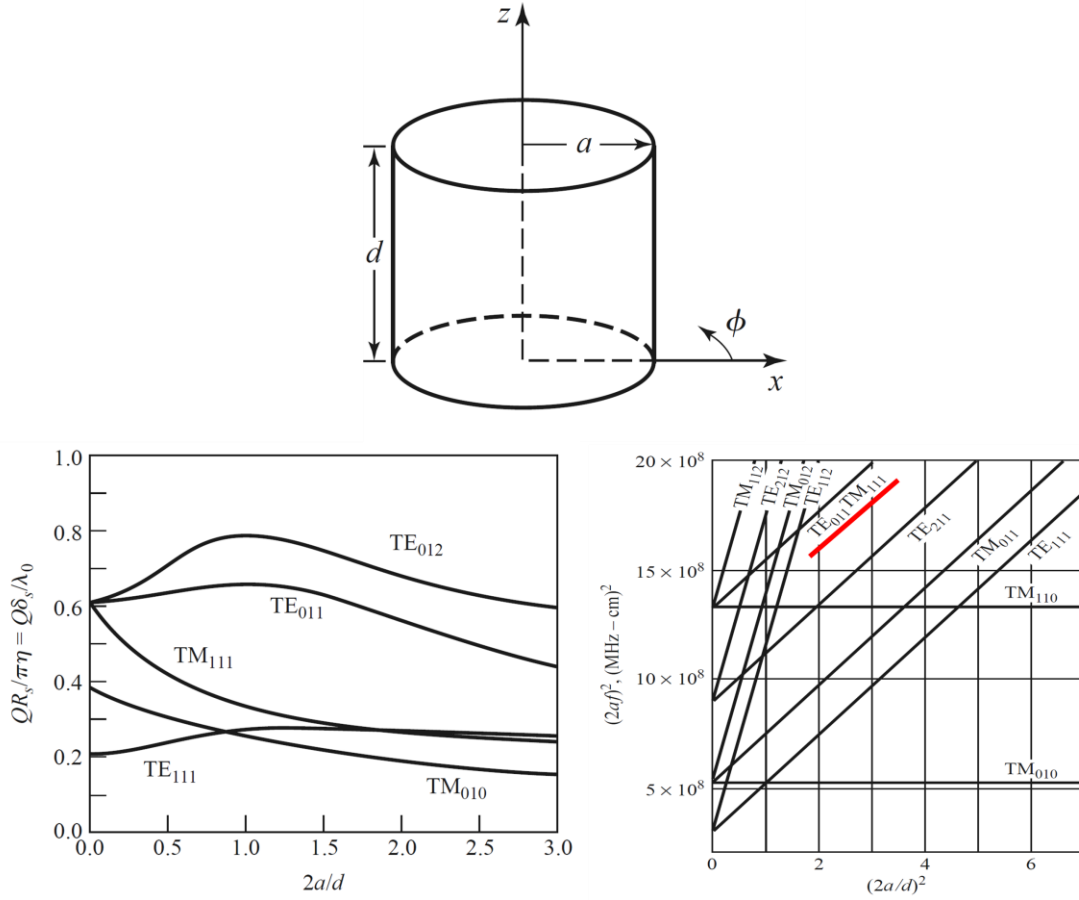


Fig. 6.2 - 2. Q factor for different modes and the mode chart for a circular cylindrical cavity. [83]

The current distributions of the  $TE_{011}$  and  $TM_{111}$  modes of a cylindrical cavity resonator are shown in Fig. 6.2-3. As can be seen, the current distribution of the  $TE_{011}$  mode is nearly zero at the center and at the edges of the top and bottom covers. On the other hand, the current distribution of  $TM_{111}$  mode is very strong at the center as well as at the edge of the top and bottom covers. By taking advantage of the differences in the current distribution of these two modes, several techniques have been developed to separate the  $TM_{111}$  mode from the  $TE_{011}$  mode.

Currently, three main techniques are used to split the  $TM_{111}$  mode: shaping the cavity sidewall [65], adding metallic posts on the cavity end walls [84], and designing the end walls with a perimeter channel and center bore [66]. Of these three technologies, shaping the sidewall of the cavity is the most effective method to separate the  $TM_{111}$  mode from the operating  $TE_{011}$  mode. In [65], a barrel-shaped cavity resonator was reported, as illustrated in Fig. 6.2-4. However, it is difficult to fabricate the inclined portion of the sidewall (highlighted in red) using the DRIE process; moreover, the slope of the inclined portion cannot be controlled. In order to use the DRIE process

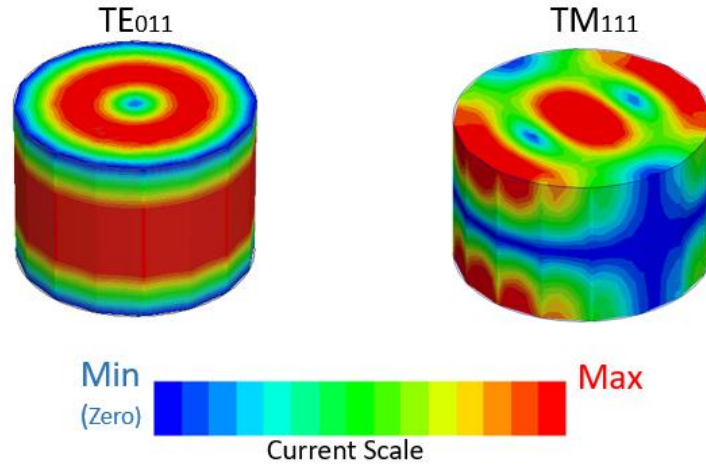


Fig. 6.2 - 3. Current distribution for the TE<sub>011</sub> mode and TM<sub>111</sub> mode of a circular cylindrical cavity.

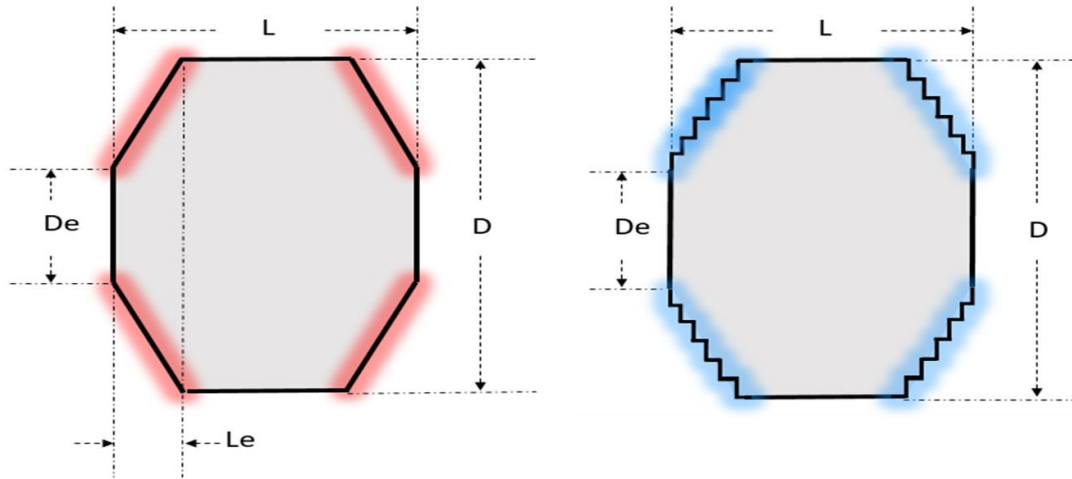


Fig. 6.2 - 4. The schematics of the published barrel-shaped cavity resonator in [65] and the proposed cavity resonator with stepped inclined sidewalls.

to implement a barrel-shaped cavity resonator on a silicon wafer, a stepped inclined sidewall is proposed, as highlighted in blue in Fig. 6.2-4.

Figure 6.2-5 presents eigenmode simulations of a cylindrical cavity resonator and a proposed stepped inclined sidewall cylindrical cavity resonator. Both cavities are filled with air, and silver is used as a conductor. The simulation shows that the TM<sub>111</sub> mode is separated from the TE<sub>011</sub> mode by a band of 4.7 GHz. In addition, the TE<sub>011</sub> mode has a Q of 9,794. Figure 6.2-6 shows the eigenmode simulation of a cylindrical cavity resonator with four silver posts (in black) added to the cavity end wall, which applies the method introduced in [84]. As can be seen, the TM<sub>111</sub> modes

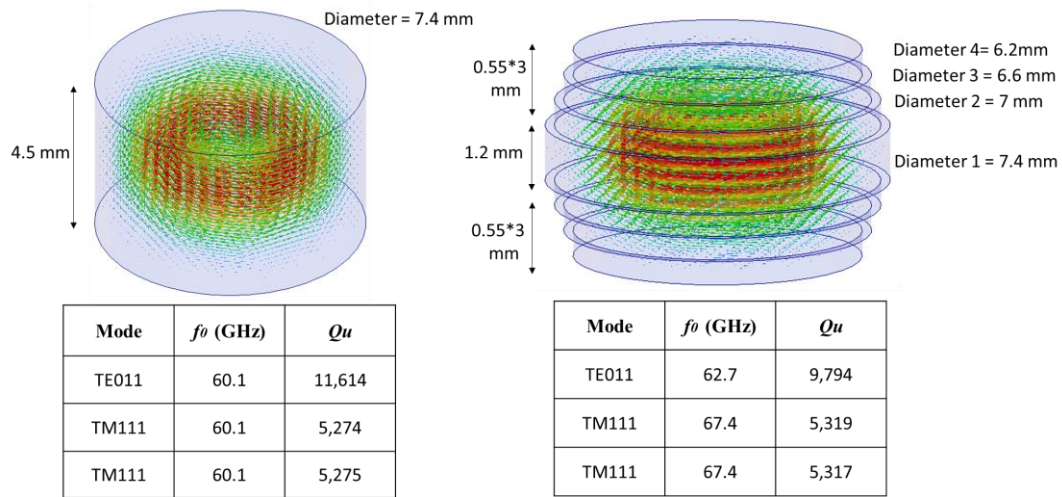


Fig. 6.2 - 5. Simulations of a cylindrical cavity resonator and a proposed stepped inclined sidewall cylindrical cavity resonator.

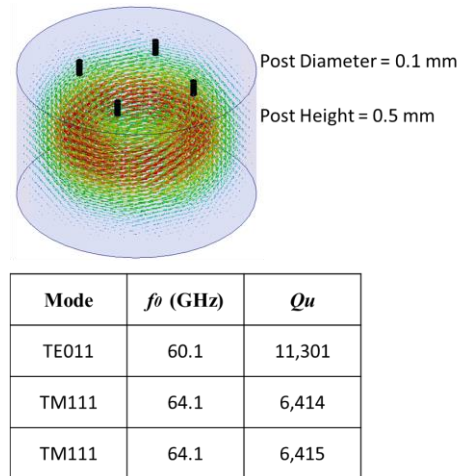


Fig. 6.2 - 6. Simulation of a cylindrical cavity resonator with four silver posts.

are split from the  $TE_{011}$  mode by 4 GHz, which is smaller than the separation, by shaping the cavity sidewalls as depicted in Fig. 6.2-5. However, the  $Q$  factor is 1,500 higher.

Figure 6.2-7 illustrates the 3D layout and layer-by-layer view of a  $TE_{011}$  mode barrel-shaped cavity resonator filter. Layers 1 to 8 are fabricated by etching through standard 4-inch Si wafers with DRIE technology, and the etched-through Si pieces are then coated with 3  $\mu\text{m}$  thick gold. The input/output (I/O) ports and the top cover of the filter are built on the front and back sides of a 254  $\mu\text{m}$  thick alumina substrate, respectively. This filter is designed at the center frequency of 61.9 GHz with a fractional bandwidth of 0.3%. The responses of the filter are shown in Fig. 6.2-8. The dimension of this filter is provided in Fig. 6.2-9 and Fig. 6.2-10.

To excite the  $TE_{011}$  mode of the cylindrical cavity resonator, an opening is created on the cover of the resonator, as shown in Fig. 6.2-11. This is the backside of the alumina substrate. Further, the opening can be looked as a  $3\text{ }\mu\text{m}$  long rectangular waveguide with its  $TE_{10}$  mode excited, with the ridges in the opening structure being used for better impedance matching. On the top side of the alumina substrate, the microstrip line and a  $50\text{ }\Omega$  GCPW line are used as the I/O ports. The designed I/O ports allow the filter to be surface mountable. The inter-resonator couplings are realized by using the rectangular waveguide that is operating in the  $TE_{10}$  mode, as shown in Fig. 6.2-12.

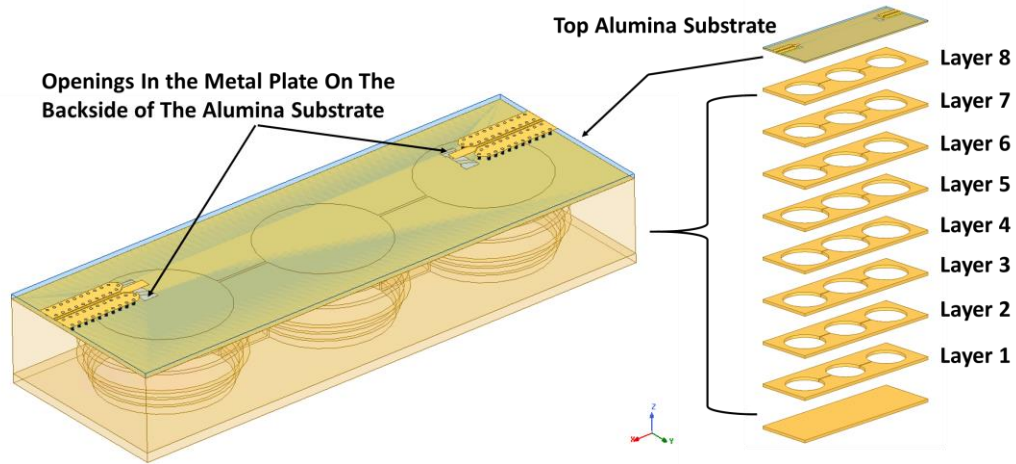


Fig. 6.2 - 7. The 3D view and the layer-by-layer view of a stepped inclined sidewall cylindrical cavity resonator filter.

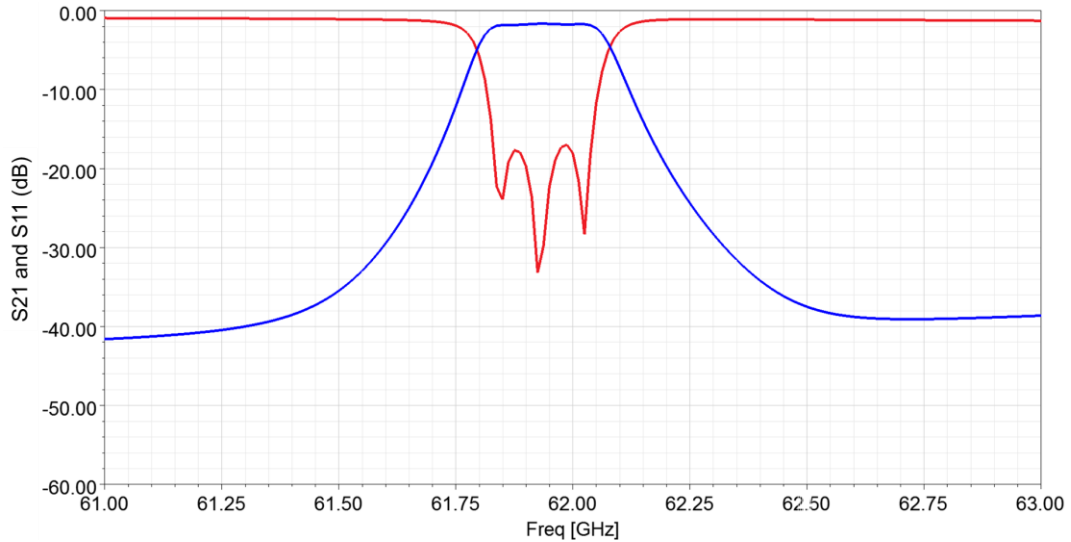


Fig. 6.2 - 8. The simulation results of a stepped inclined sidewall cylindrical cavity resonator filter.

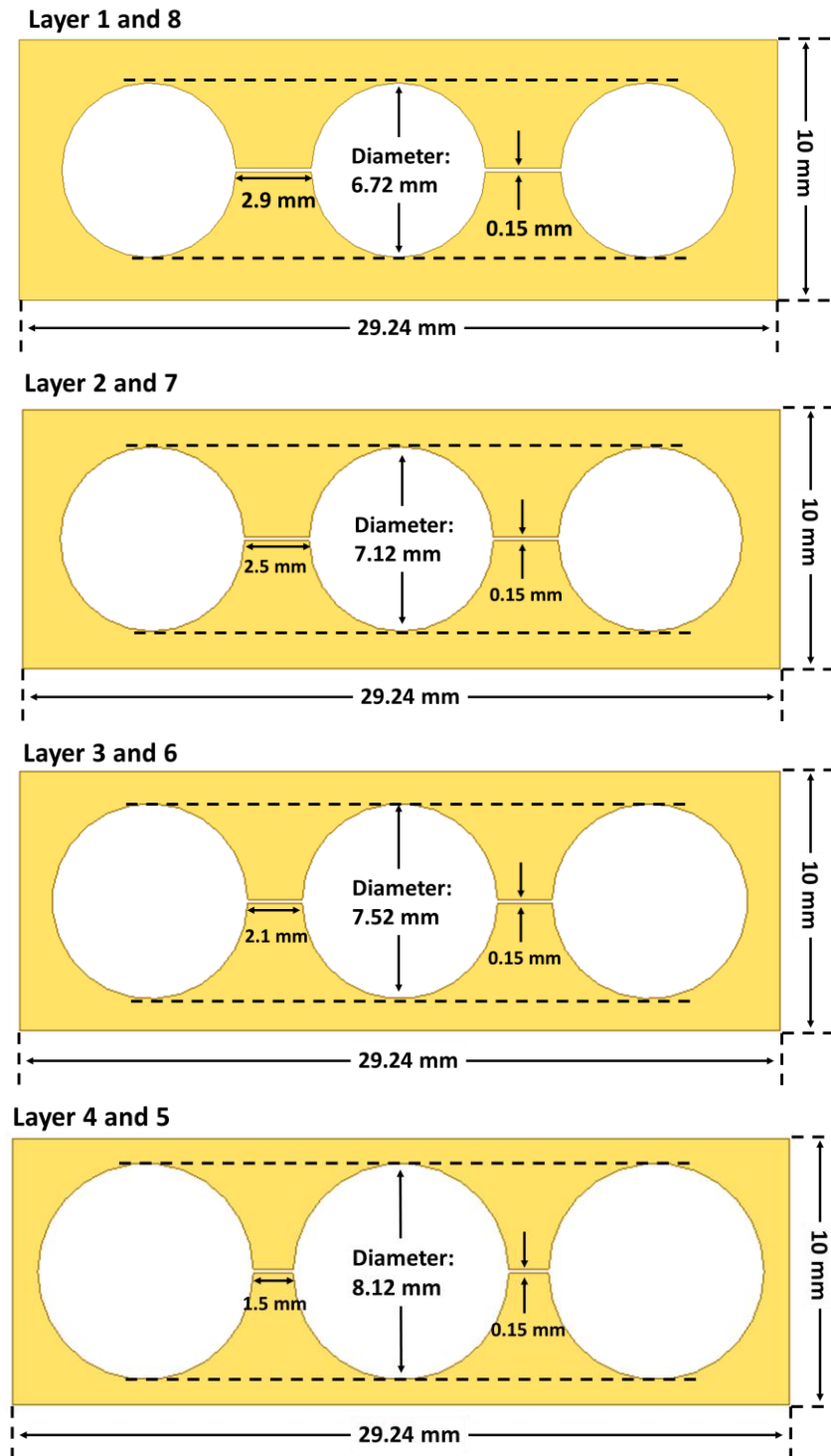
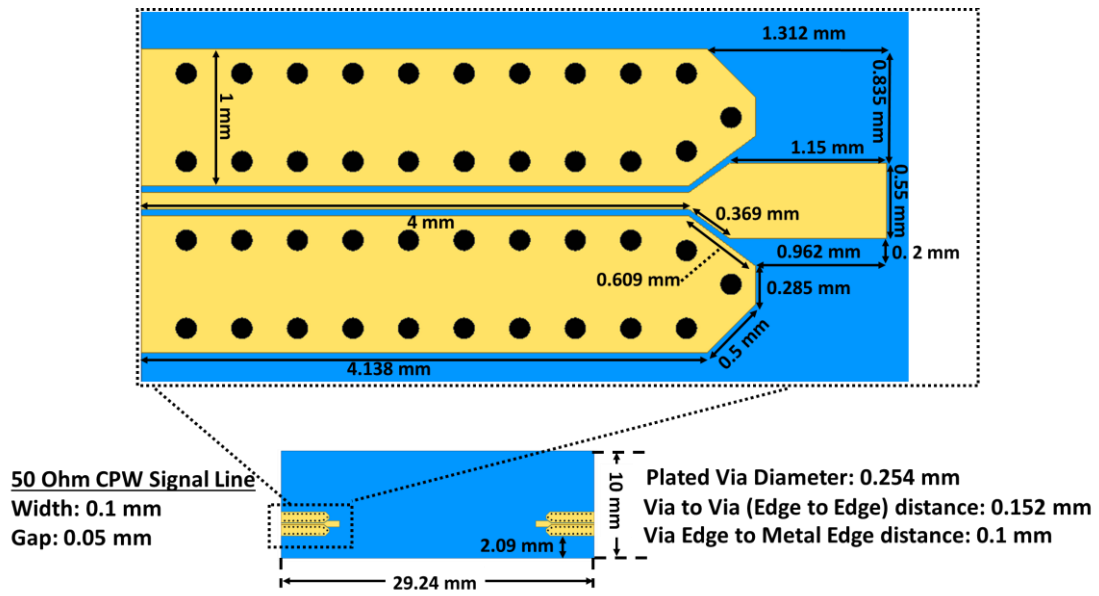
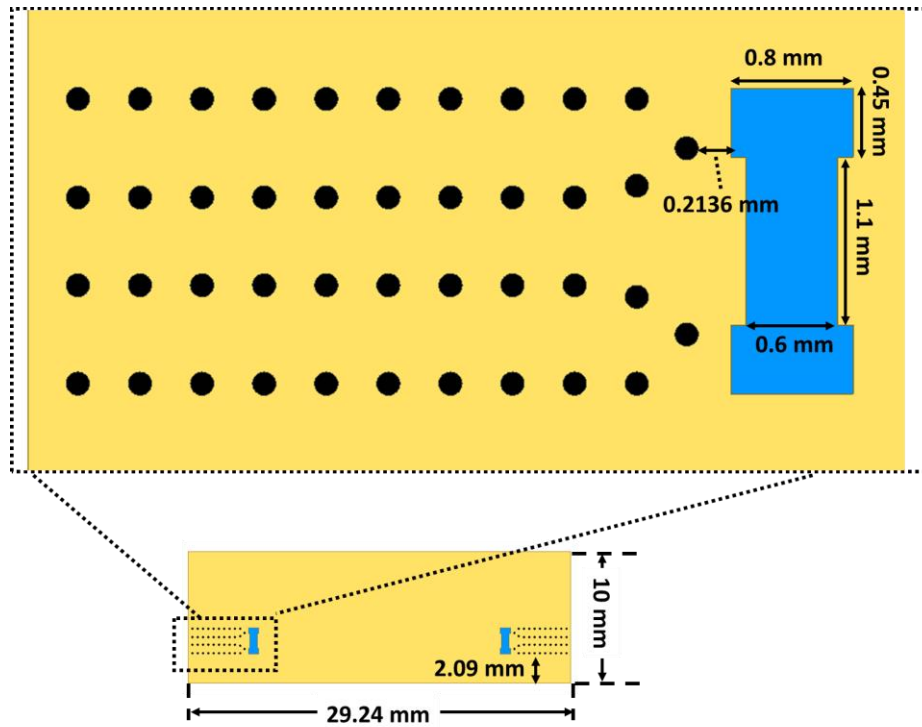


Fig. 6.2 - 9. The dimensions of the cavity structures for the stepped inclined sidewall cylindrical cavity resonator filter built on Si wafers.





(a)



(b)

Fig. 6.2 - 10. The dimensions of the input/output of the stepped inclined sidewall cylindrical cavity resonator filter.



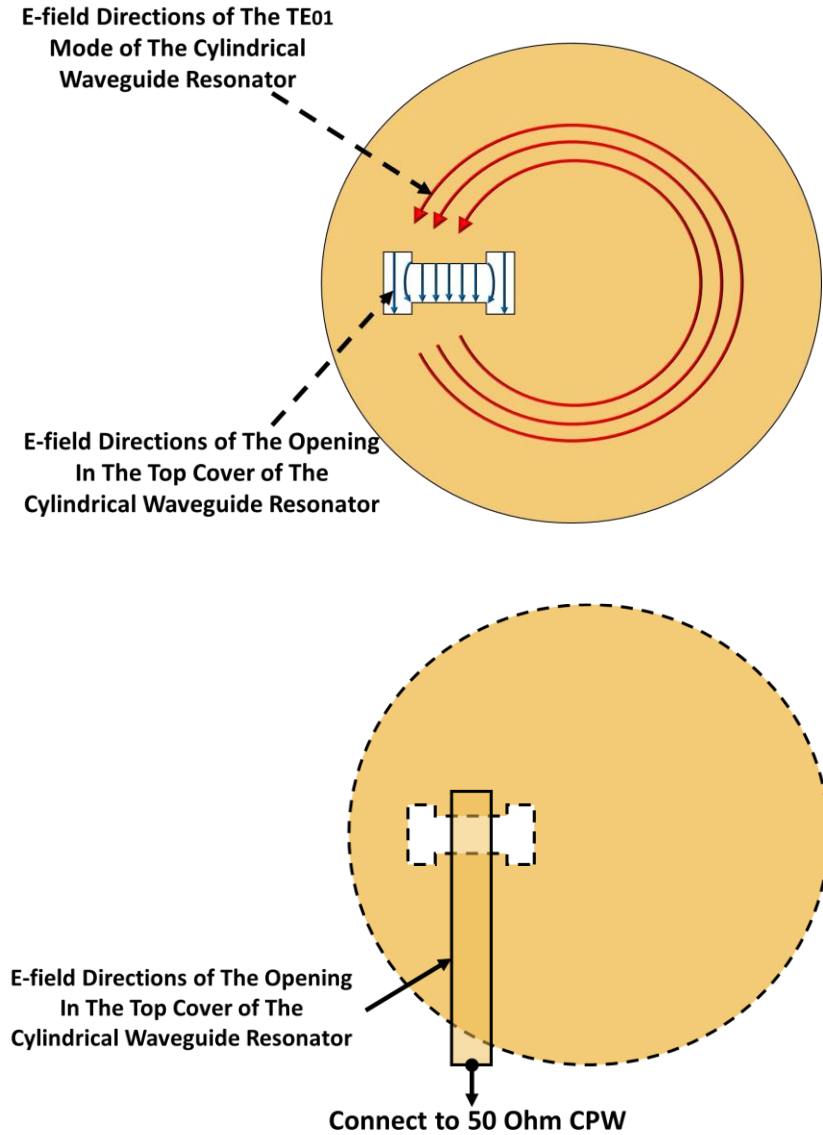


Fig. 6.2 - 11. A defected ground microstrip line is used to excite the TE<sub>01</sub> mode of a cylindrical cavity resonator.

As discussed above, the TE<sub>011</sub> mode barrel-shaped cavity resonator filter has very-high- $Q$  values at mm-Wave frequencies, while circumventing the issue of the degenerate TM<sub>111</sub> mode. The advantage of this structure become more pronounced as the operating frequencies increase to several hundreds of gigahertz or even terahertz. Figure 6.2-13 shows a two-pole TE<sub>011</sub> mode cylindrical cavity filter designed at the center frequency of 229.4 GHz with an ultra-narrow fractional bandwidth of 0.1%. The EM simulation results indicate that the insertion loss level within the passband is less than 1.2 dB, which corresponds to a  $Q$  value of 3,700, and this will make the proposed ultra-high- $Q$  filter potentially useful for sub-THz and THz applications.

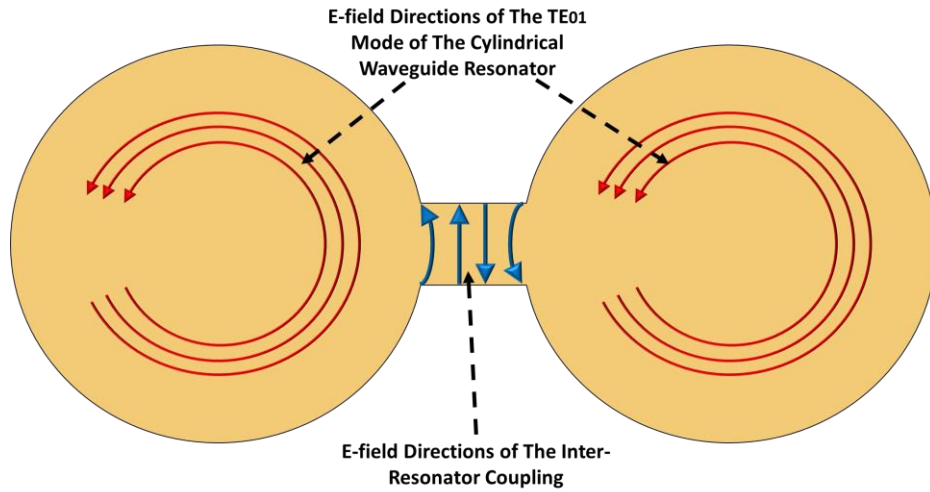


Fig. 6.2 - 12. The inter-resonator coupling between two cylindrical cavity resonators can be realized by using a rectangular waveguide.

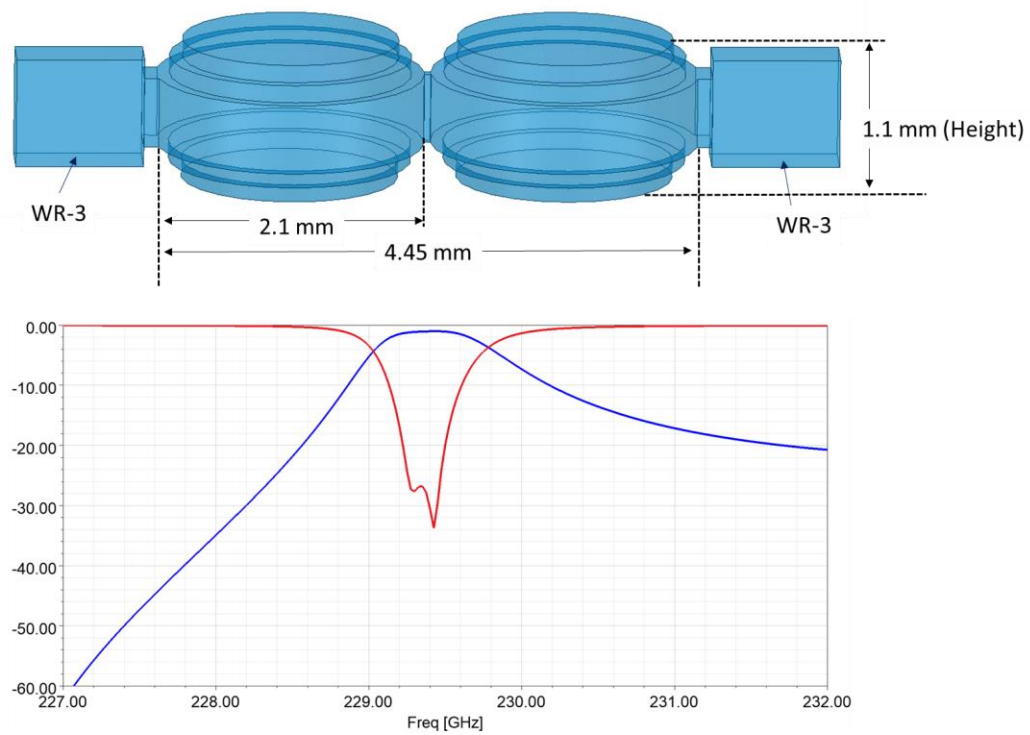


Fig. 6.2 - 13. A very-high-Q TE<sub>011</sub> mode cylindrical cavity filter is designed at the center frequency of 229.4 GHz with a fractional bandwidth of 0.1%.

## 6.3 Fabrication of Si-Micromachined Filters

The micromachining fabrication process shown in Fig. 6.3-1 was used to fabricate the cavities for the T-septum filters designed in section 6.1. First, the Si wafer was cleaned by using the standard RCA cleaning process. Then, a 15  $\mu\text{m}$  thick photoresist (AZ®P4620) layer was coated on the cleaned Si wafer with the edge bead removed (Fig. 6.3-2) by using the Brewer Cee®200X Precision Spin Coater at the Quantum-Nano Fabrication and Characterization Facility (QNFCF) at the University of Waterloo. Next, the photoresist layer was patterned by employing the Heidelberg MLA150 Maskless Aligner with a laser (405 nm wavelength) energy density of 800  $\text{mj}/\text{cm}^2$  at the QNFCF. Figure 6.3-3 shows photos of Si wafers with patterned photoresist layers used for developing T-septum filters. The DRIE process was applied by the PlasmaPro 100 Cobra® ICP Etch system at the CRIFE lab.

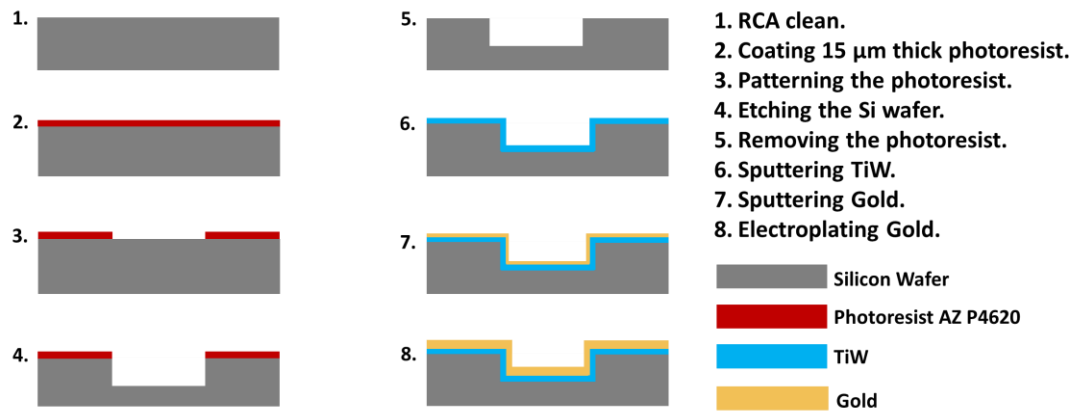


Fig. 6.3 - 1. The micromachining process was used to make cavities on Si wafers for the T-septum filters designed in Section 6.1.

Photos of the etched Si wafers used for developing T-septum filters are shown in Fig. 6.3-4. After finishing the DRIE processes, the photoresist layers on the etched Si wafers were removed and titanium-tungsten (TiW) was sputtered on the Si pieces as the adhesive layers for the following gold plating process. Then, the gold layer was sputtered on the Si pieces by using the Intlvac® Nanochrome Deposition System at the CIRFE lab as shown in Fig. 6.3-5. More details of the fabrication process can be found in Appendix B.

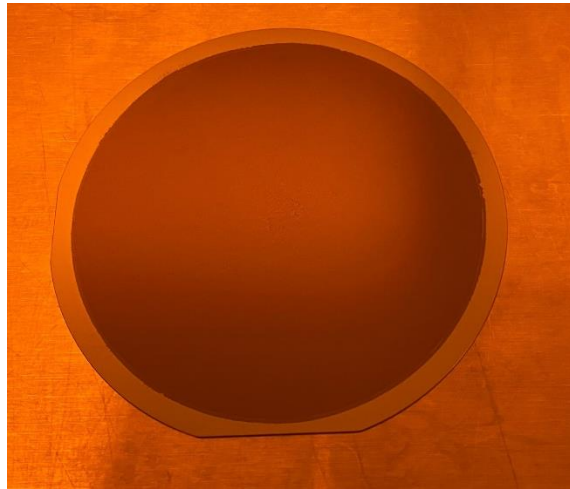


Fig. 6.3 - 2. The photo of a 4-inch Si wafer coated with 15  $\mu\text{m}$  thick positive photoresist and the edge bead is removed.

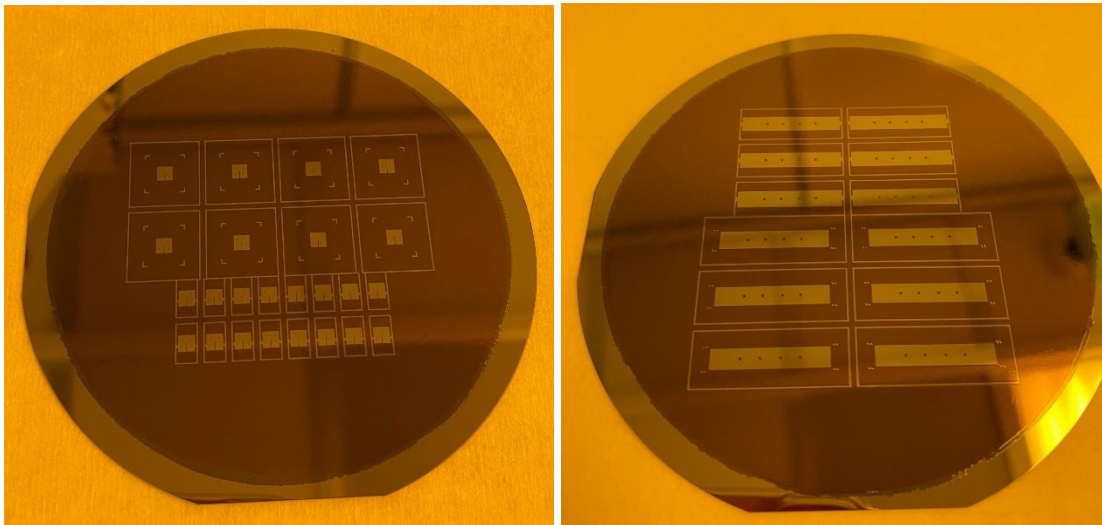


Fig. 6.3 - 3. The Si wafers with patterned photoresist layers used for developing the filter shown in Fig. 6.1-6 and Fig. 6.1-12.

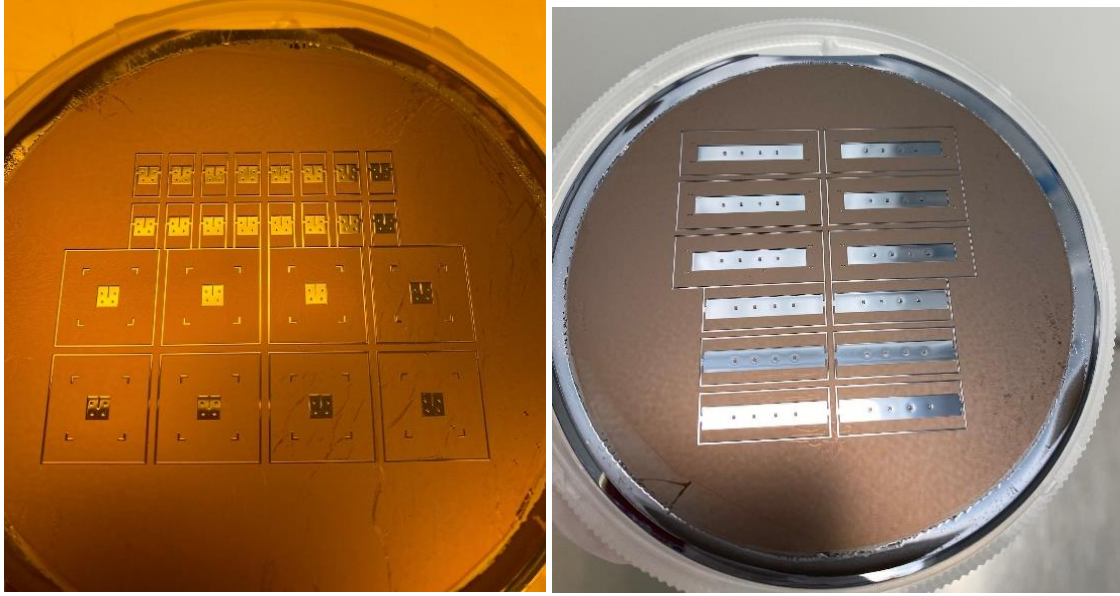


Fig. 6.3 - 4. The Si wafer shown in Fig. 6.3-3 were etched by using DRIE.



(a)

(b)

Fig. 6.3 - 5. (a) The metallized Si pieces for developing the filter shown in Fig. 6.1-6. (b) The metallized Si pieces for developing the filter shown in Fig. 6.1-12.

The micromachining fabrication process shown in Fig. 6.3-6 was used to fabricate the cavities for the barrel-shaped cavity resonator filter designed in section 6.2. To fabricate this filter, the Si wafers need to be etched through by using DRIE. Fabrication Steps 1 to 5 in Fig. 6.3-6 are the same as in Fig. 6.3-1. The metallization steps were then performed on both sides of the Si wafers, as presented in Steps 6 to 9 in Fig. 6.3.6. To etch through the Si wafer, the Si wafer was first etched

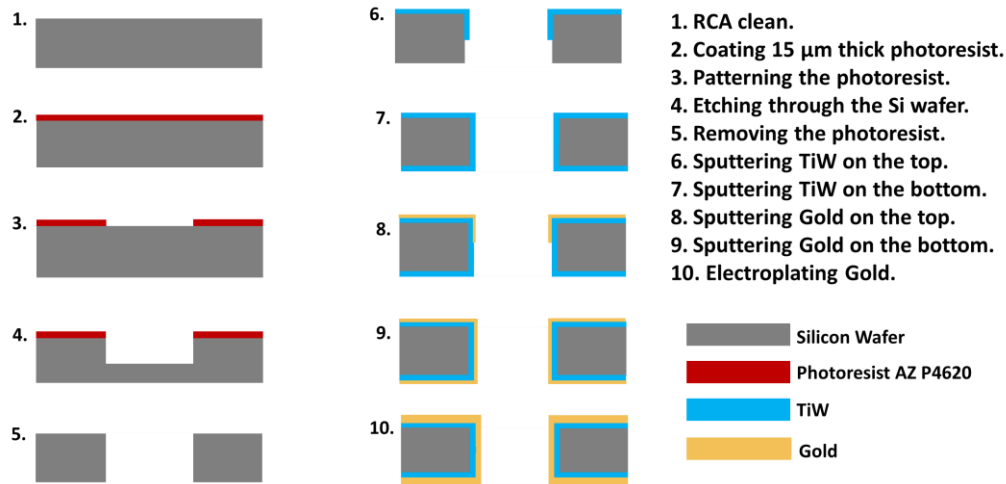


Fig. 6.3 - 6. The micromachining process was used to make cavities on Si wafers for the barrel-shape cavity resonator filter filter designed in Section 6.2.

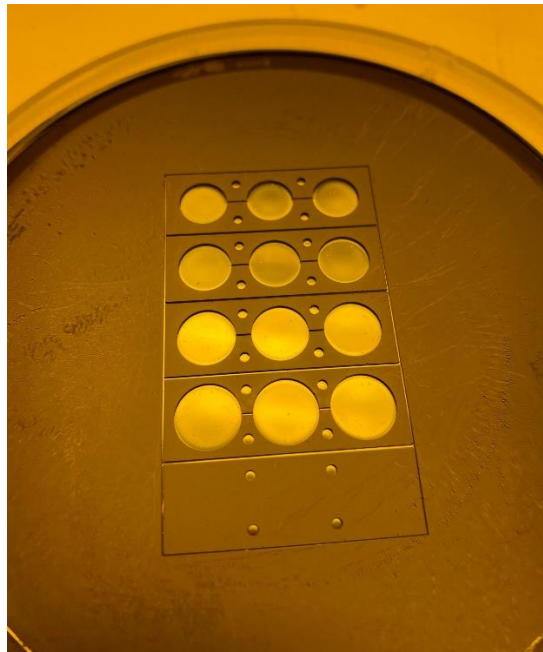


Fig. 6.3 - 7. The Si wafer was first etched by using DRIE to make the designed patterns have a depth of 400  $\mu\text{m}$ .

by using DRIE to make the designed patterns have a depth of 400  $\mu\text{m}$ , as depicted in Fig. 6.3.7. The Si wafer was then diced to a smaller Si piece, which was subsequently mounted on a carrier wafer (Fig. 6.3-8) for the final etching process (Fig. 6.3-9). Figure 6.3-10 shows the photo of the metallized etched through Si pieces.

The circuits presented in Fig. 6.1-10, Fig. 6.1-15 and Fig. 6.2-10 were built on a 10-mil thick alumina substrate, which was fabricated by the commercial thin-film service company, TecDia [85]. The photos of the fabricated alumina substrate are provided in Fig. 6.3-11 and Fig.6.3-12. The



alumina substrate was diced, enabling the designed filters to be assembled by bonding the alumina pieces with the corresponding DIRE etched Si pieces.

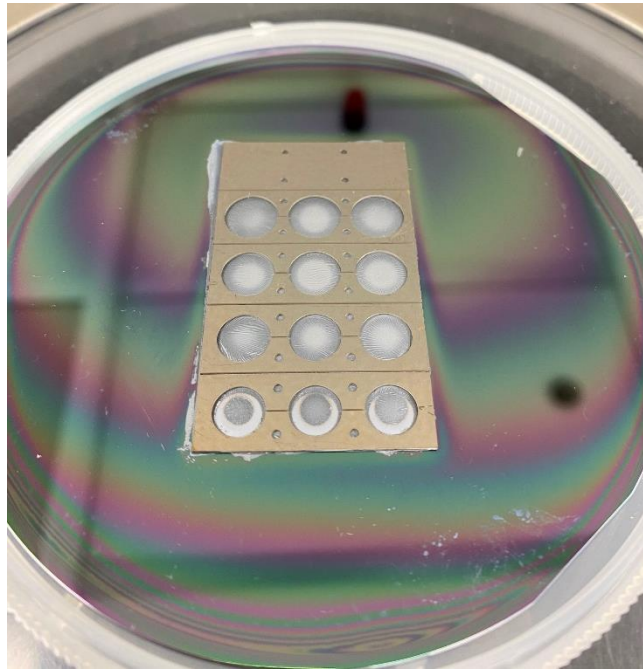


Fig. 6.3 - 8. The smaller Si piece was mounted on a carrier wafer for the final etching through process.

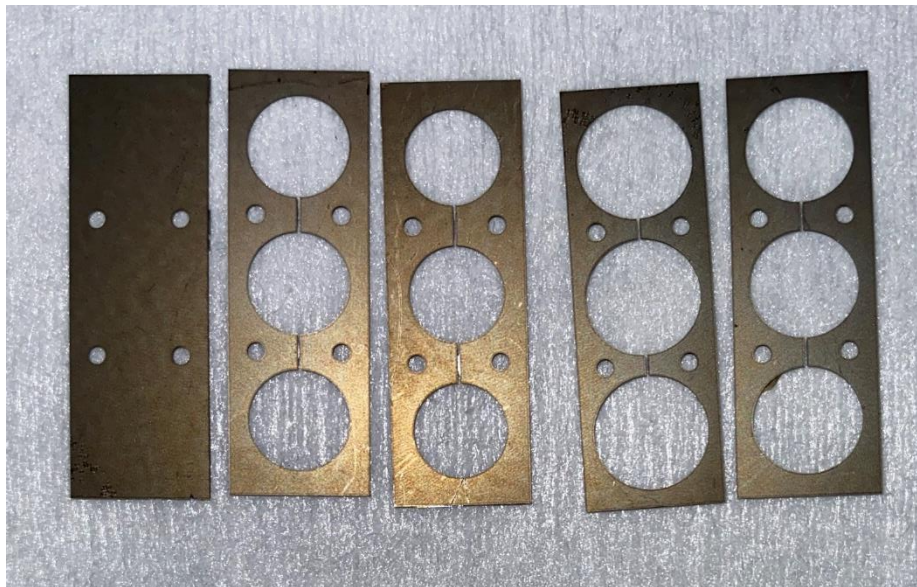


Fig. 6.3 - 9. The photo of the etched through Si pieces used for developing the barrel shape cavity resonator filter.



Fig. 6.3 - 10. The photo of the metallized etched through Si pieces.

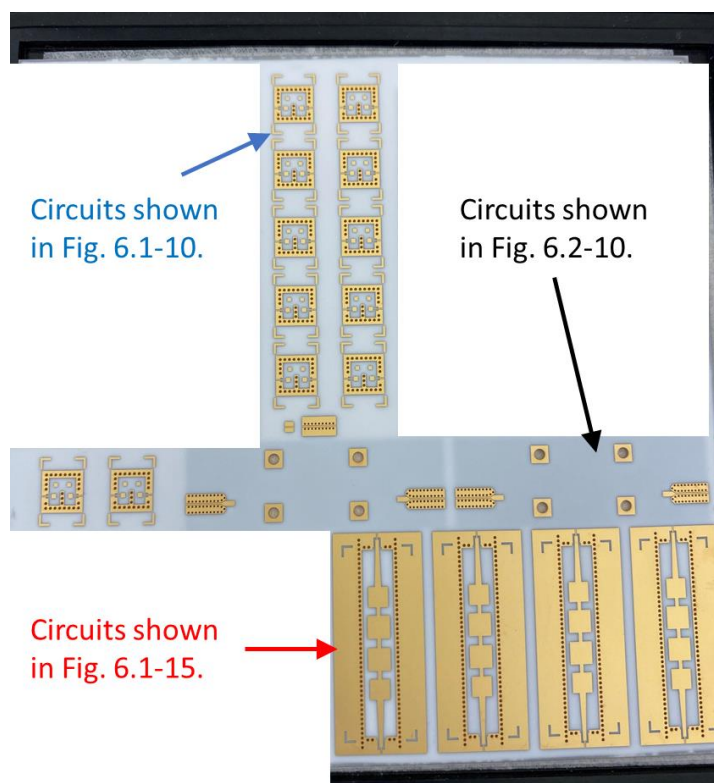


Fig. 6.3 - 11. The photo of the fabricated alumina substrate (top).



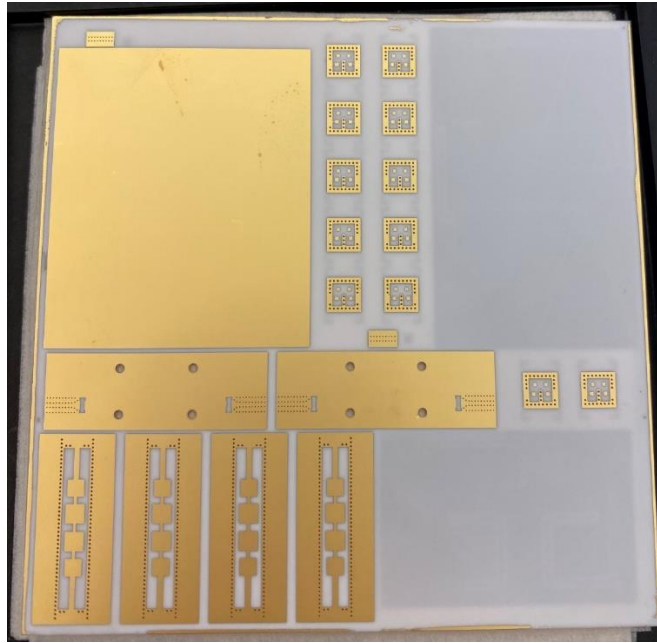


Fig. 6.3 - 12. The photo of the fabricated alumina substrate (bottom).

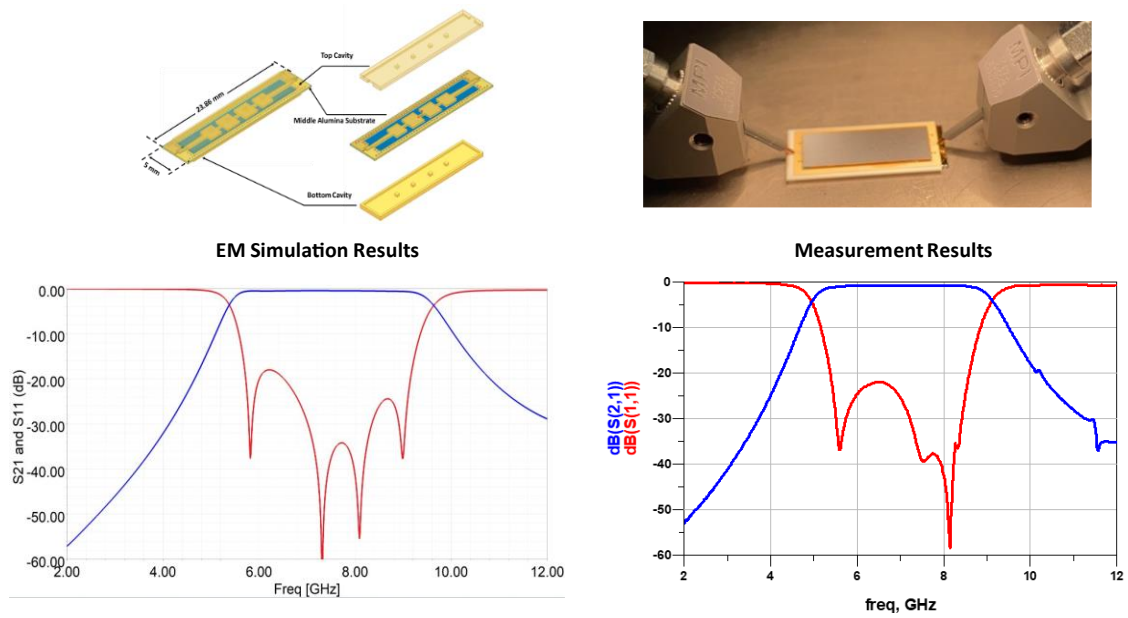


Fig. 6.3 - 13. The EM simulation and the measurement results of the micromachined dielectric-loaded wideband filter shown in Fig. 6.1-11.

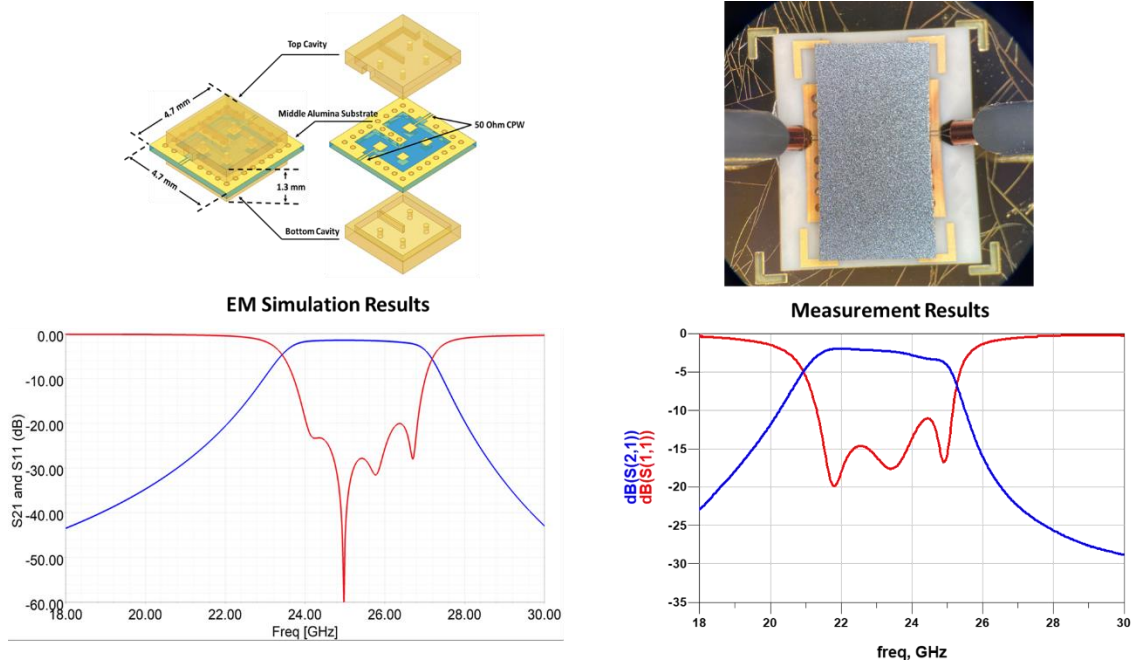


Fig. 6.3 - 14. The EM simulation and the measurement results of the micromachined dielectric-loaded wideband filter shown in Fig. 6.1-6.

The micromachined dielectric-loaded filters (Fig. 6.1-6 and Fig. 6.1-11) designed in section 6.1 were assembled by using a Tresky T-3000-FC3 Die Bonder [86] at QNFCF with epoxy (EPO-TEK® H20E) [87] as the adhesive. The measurement results of the filters are provided in Fig. 6.3-13 and Fig. 6.3-14. The deviations of the measurement responses are mainly caused by the use of the thick epoxy layers. As illustrated in Fig. 6.3-15, the epoxy was manually applied on the Si pieces, which increases the height of the filter. Moreover, the epoxy has a low conductivity, which increases the insertion loss. Figure 6.3-16 shows the simulation results of the filter by sweeping the thickness of the epoxy layers. As can be seen, the center frequency of the filter decreases and the insertion loss degrades as the epoxy thickness increases. When the thickness of the epoxy is 50  $\mu\text{m}$ , the center frequency, the insertion and return loss levels of the simulation results shown in Fig. 6.3-16 match the measurement results shown in Fig. 6.3-14. To improve the performance of the fabricated filters, gold-to-gold compression bonding technology needs to be used to assemble filters. The surface roughness of the metal layer, especially the metal surface roughness of the DRIE micromachined cavity sidewalls, also causes more insertion loss. The surface roughness of the DRIE micromachined cavity sidewalls may be improved by using the method shown in Fig. B.3-6 in the appendix. Moreover, the simulations were carried out assuming a typical loss tangent of the alumina that is quoted by the suppliers, which is typically characterized at low frequency. No data available from the supplier on loss tangent value at millimeter-wave frequencies. Since the loss

tangent is proportional to the frequency, the increment of the loss tangent at higher frequencies also leads to the offsets in the center frequency and the insertion loss level.

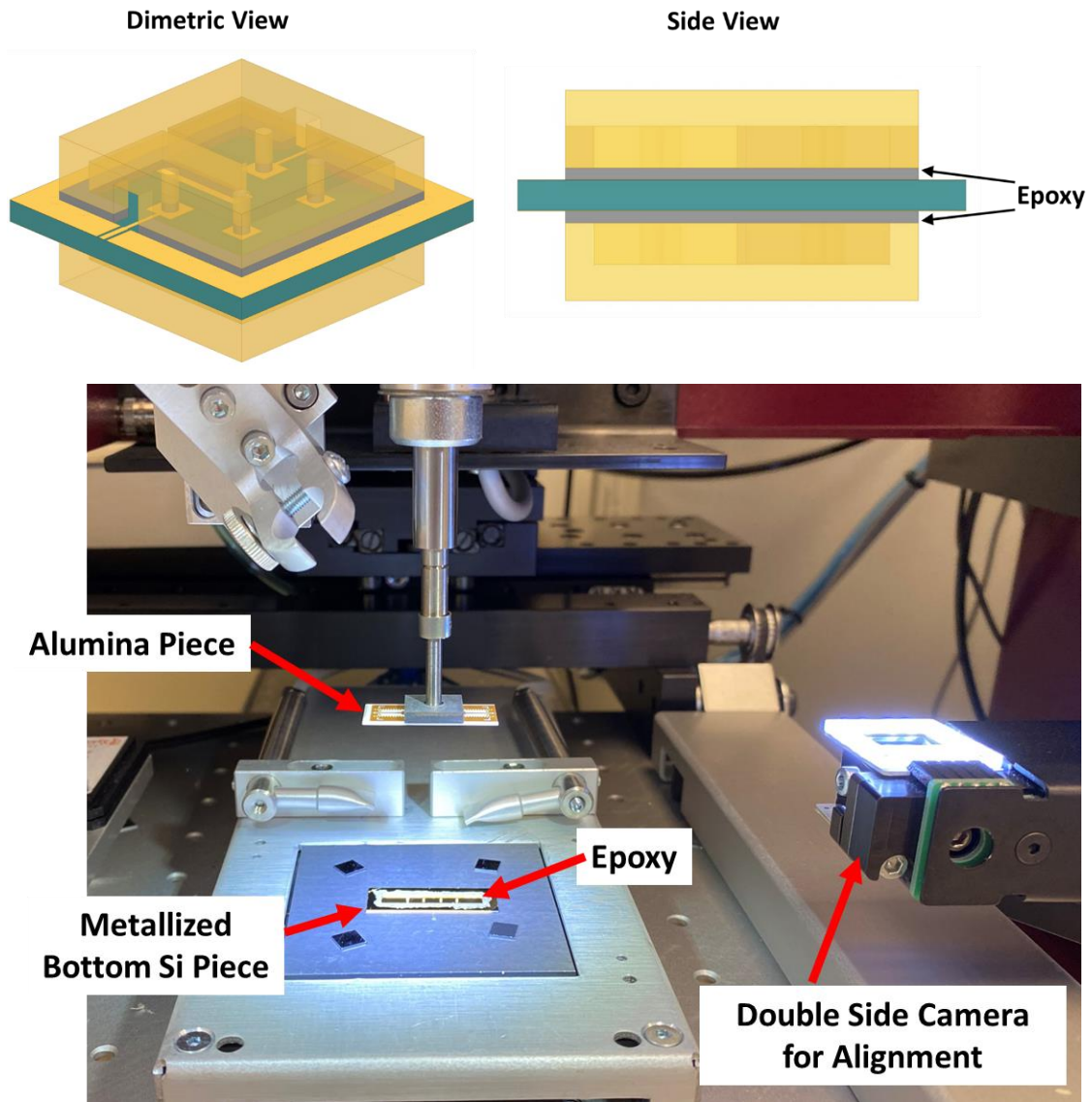


Fig. 6.3 - 15. The micromachined dielectric-loaded filters were assembled by using a Tresky T-3000-FC3 Die Bonder [86] with epoxy (EPO-TEK® H20E) as the adhesive

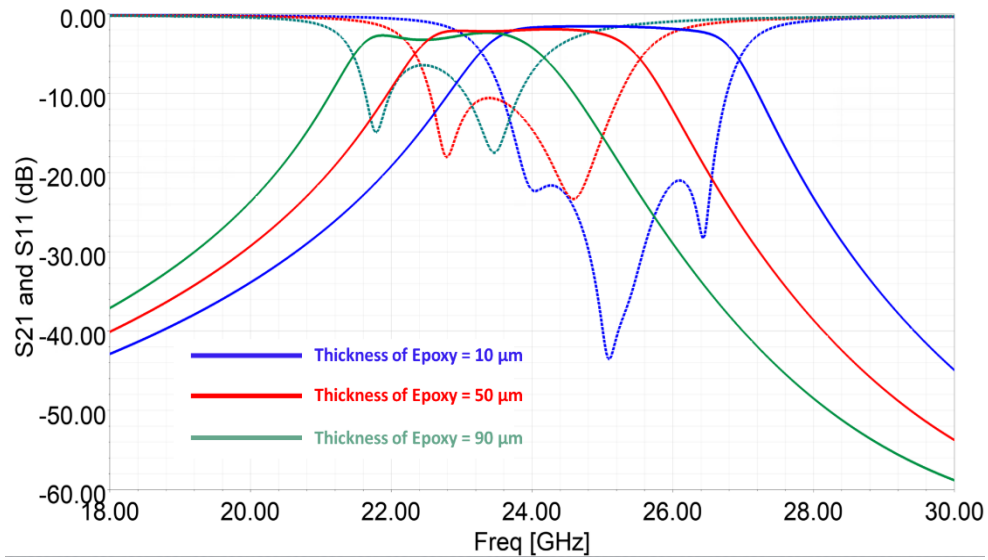


Fig. 6.3 - 16. The EM simulations results demonstrate the effect of the thickness of epoxy thickness affects the filter performance significantly.

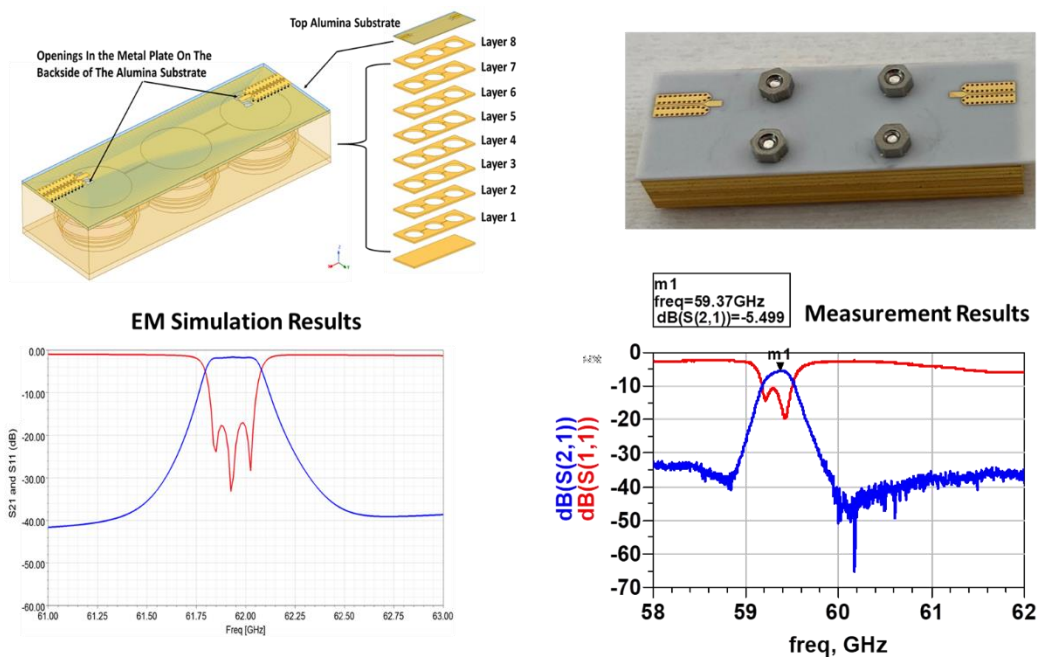


Fig. 6.3 - 17. The EM simulation and the measurement results of the micromachined barrel-shape cavity resonator filters shown in Fig. 6.2-7.

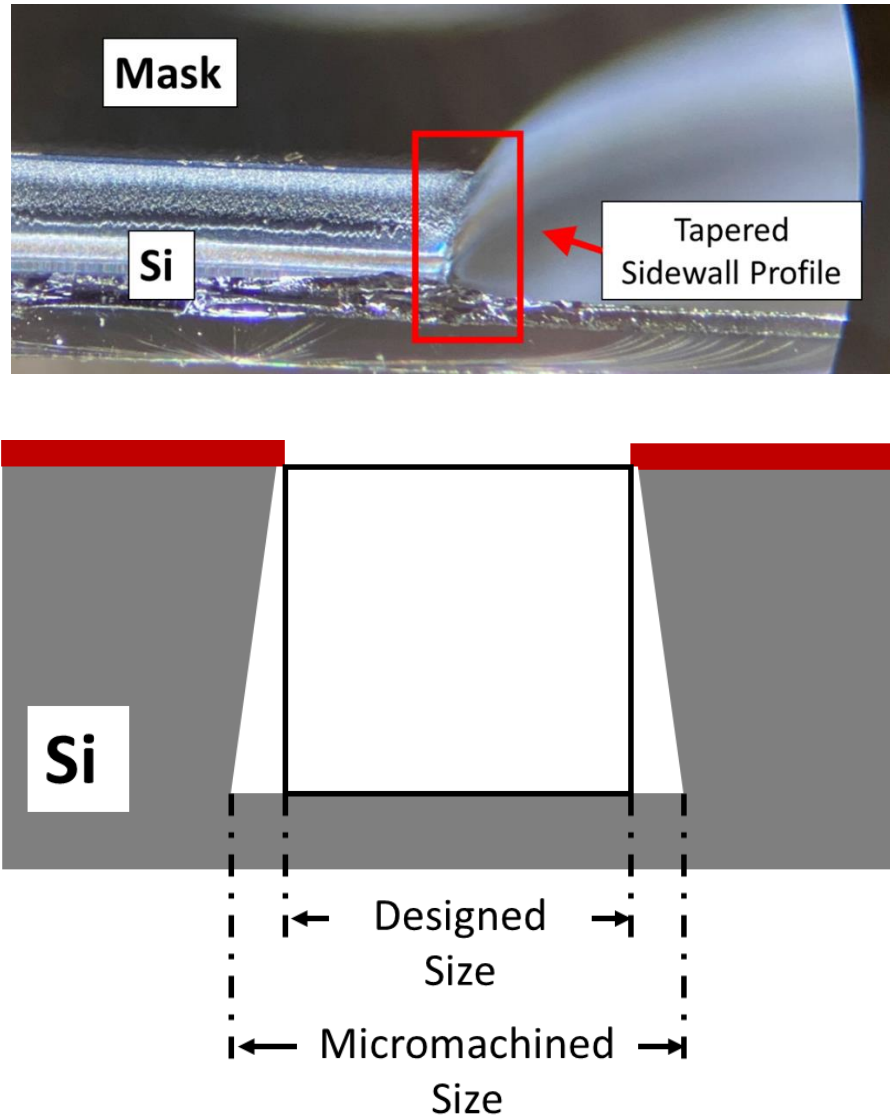


Fig. 6.3 - 18. The photo and the schematic of the cross-section of the DRIE micromachined silicon trench.

The micromachined barrel-shape cavity resonator filters (Fig. 6.2-7) designed in section 6.2 were assembled with 4 screws and measured as shown in Fig. 6.3-17. The simulation was carried out assuming perfect vertical cavity sidewall profiles. The simulated center frequency of the filter is at 61.9 GHz, while the measured center frequency is 60 GHz. The center frequency offset is mainly due to the taper angle of the DRIE micromachined cavity sidewall profile, which results in the micromachined cavities has larger diameters than the designed ones as illustrated in Fig. 6.3-18. This is one of the most challenging problems of using DRIE to realize nearly perfect vertical cavity sidewalls for etching superdeep (deeper than 300  $\mu\text{m}$ ) and large-opening (wider than 500  $\mu\text{m}$ ) structures [23]-[25] [88]-[90]. As illustrated in Fig. 6.3-19, the simulation results show the center frequency shift to around 60 GHz with the designed radiuses increased by 200  $\mu\text{m}$ , which is around

5 percent of the designed ones. Recently, [90] proposes a process to circumvent this problem and demonstrates encouraging results. The new technique proposed in [90] can be applied to improve the performance of the micromachined barrel-shape cavity resonator filter for future work. The insertion and return loss degradations in the measured results are caused by the adhesion. In order to improve the insertion and return loss of the fabricated filter, it is necessary to use gold-to-gold compression bonding technology to assemble the filter. In addition, the simulation assumes that the gold is perfect smooth, but the sidewalls of the DRIE micromachined cavities are not. The rough sidewall of the DRIE micromachined cavity is an inherent consequence of the Bosch process, because the anisotropic etching is achieved by alternatively switching the etching and passivation steps. To smooth the sidewall, the post-DRIE process illustrated in Fig. B.3-6 can be employed. Electroplating is also necessary to ensure that the thickness of the gold layer on the sidewall is at least three times higher than the skin depth, because it is very difficult and expensive to use sputtering technology to obtain a gold layer with a thickness of more than 1  $\mu\text{m}$  on the cavity sidewall (the skin depth of gold at 60 GHz is 0.308  $\mu\text{m}$ ).

As discussed in this section, the most challenging parts of successfully developing micromachined 3D structure filters are the packaging processes. With the acquirement of state-of-the-art packaging and assembly equipment, as more and more scientific research efforts are invested in this field, the DRIE technology will play a pivotal role in developing high quality mm-Wave RF filters.

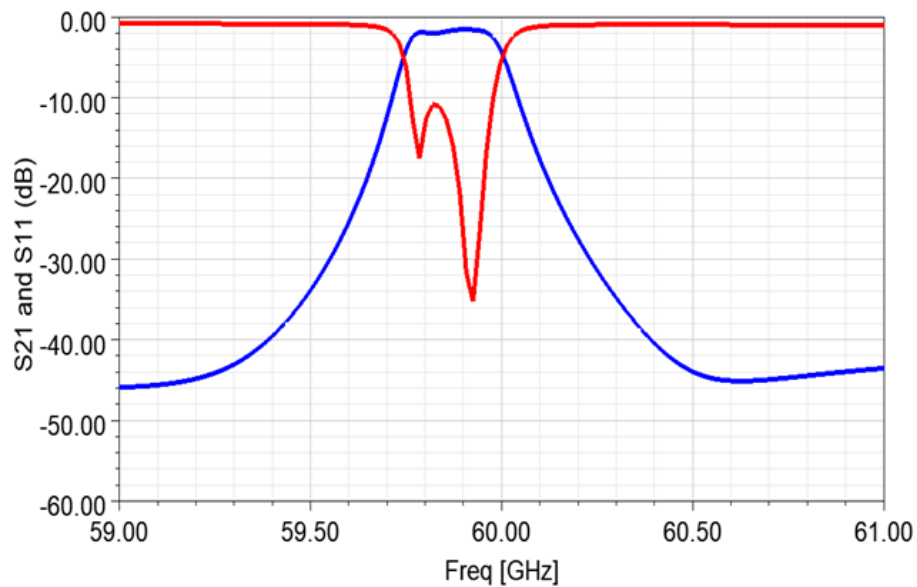


Fig. 6.3 - 19. The EM simulation results of the micromachined barrel-shape cavity resonator filters shown in Fig. 6.2-7 with the radiuses shown in Fig. 6.2-9 increased by 200  $\mu\text{m}$ .



# Chapter 7

## Conclusion and Future Work

### 7.1 Contributions

The main focus of this thesis was on the development of high- $Q$  filters for mm-Wave applications by using the Nb-based superconducting technologies and silicon-micromachining through the use of the DRIE techniques.

Chapter 3 introduced a new sequential filter design and tuning method that employs a phase of the input impedance (PII) as the design parameter. The novel approach was shown to require much less computation time than previous methods, since the distinguishing information about the offsets in resonant frequencies and inter-resonator couplings can be acquired easily from the phase response of the input impedance. Closed-form expressions for the phase transition locations were provided. The method was then applied in designing an ultra-wideband filter, a narrowband 4-2 quasi-elliptic filter, and a wideband diplexer. Furthermore, the PII response was used to extract the equivalent electrical length of the unknown transmission line caused by the non-ideal filter physical I/O ports. Finally, the effect of finite  $Q$  was discussed, and an alternative design parameter response was proposed for dealing with the design and tuning of very low- $Q$  filter.

In Chapter 4, a highly miniature 8-pole multi-layer niobium-based superconducting mm-Wave UWB bandpass filter with operating frequencies from 30 GHz to 60 GHz was demonstrated. Crossovers embedded in the multilayer were employed to provide extra capacitance loading in order to achieve miniaturization and to help in fine-tuning the filter performance. Moreover, a mm-Wave UWB superconductor contiguous triplexer with a coverage of 20 GHz to 80 GHz was also designed. The triplexer has a miniature physical size of  $2.5 \text{ mm} \times 3.6 \text{ mm}$ , which allows it to be monolithically integrated with the Nb-based superconductor ADC circuits on a single chip. The design considerations and challenges for developing the mm-Wave ultra-wideband triplexer were discussed. Methods and design strategies used to develop the triplexer were also introduced. As well, a broadband 50 Ohm matched load operating from DC to 90 GHz was developed. The feasibility of integrating the mm-Wave superconductor triplexer on an MCM substrate and interfacing it with 100 GHz 1 mm commercial connectors was investigated.

In Chapter 5, a switchable band reject filter with a novel switching mechanism was introduced using a unique feature of spiral inductors designed intentionally with high parasitic capacitance. It was shown in the chapter that such a spiral inductor performs as an inductor when its metal traces are made of high conductivity metals, whereas it performs as a capacitor when its metal traces are made of low conductivity metals. A switchable band reject filter made of niobium operating at 4K was used to demonstrate the concept, with switching obtained through the use of a DC current. While the concept has been applied to a niobium superconductor spiral inductor, the same concept can potentially be employed in other types of materials whose conductivity can be switched from high to low values through triggering by electrical, thermal, or optical means.

Chapter 6 presents filter designs composed of a miniature micromachined dielectric loaded double T-septum resonator filter. The proposed filter designs provide highly compact physical size with reasonable high- $Q$  values and can be easily fabricated by using the DRIE technology. Finally, an ultra-high- $Q$  mm-Wave micromachined cavity filter with a barrel-shape was developed. The cavity operates in the high- $Q$   $TE_{01}$  mode, while spacing away the spurious that is generated from the  $TM_{11}$  mode. This filter design can be potentially useful for sub-THz and THz applications.

## 7.2 Future Work

There are several related research problems in this field that need to be explored in the future.

- The current coupling matrices synthesis technologies widely used today assume that the coupling coefficients are frequency invariant (i.e., constant). However, it is well-known that inter-resonator couplings vary with frequency in a physical filter structure. Therefore, the constant coupling matrices works efficiently only when used to describe the physical filter realizations of narrow and moderate bandwidth. Until recently, several publications have reported on the development of coupling matrices for wideband filters with frequency-dependent coupling coefficients, demonstrating encouraging progresses. Therefore, it still needs to invest more research efforts in developing frequency-dependent coupling matrices for ultra-wideband filter designs.
- Exploring the switchable spiral inductors with phase changing materials (PCM), such as  $VO_2$  (Vanadium dioxide) and GeTe (germanium telluride).
- As the operating frequencies increase above 100 GHz, the Nb-based planar superconductor filters presented in this thesis will have very low- $Q$  values. The DRIE



micromachined filters introduced in Chapter 6 can be potentially integrated with the superconductor ADC on a single chip.

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# Appendix A Measurement with the Cryogenic RF Probe Station at 4K

In order to make Nb operate at the superconducting state, Nb-based RF chips need to be cooled down below Nb's critical temperature. In this thesis, all cryogenic measurements are performed using a Lakeshore Cryogenic Probe Station. Figure A.1-1 depicts a schematic of the cryogenic chamber of the Lakeshore cryogenic probe station. The tested Nb-based RF chip can be mounted on the sampler holder by using adhesive or it can be physically clamped on the wafer holder.

In [91], different mounting approaches are analyzed and compared. As shown in [88], the best mounting approach is using silver paint [92] to semi-permanently mount the tested chip on the wafer holder, since the silver paint has a superior thermal conductivity of 429 W/mK. To use this mounting approach, silver paint needs to be manually applied to the wafer holder first, and then the tested chip is dropped on the silver paint, as shown in Fig. A.1-2. Finally, the wafer holder is baked in the oven at 100°C for 10 minutes to make the solvent in the silver paint totally evaporate. In this way, the tested chip is semi-permanently mounted on the wafer holder.

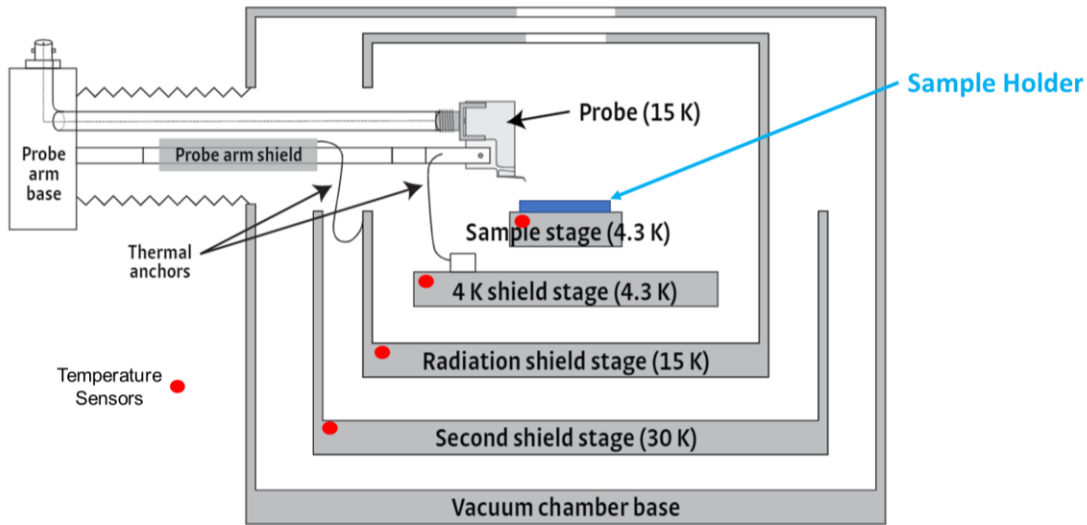


Fig. A.1 - 1. The schematic of the four thermal shields of the Lakeshore cryogenic chamber. [51]

Note that it is important to use the correct amount of silver paint while mounting the chip on the wafer holder. Too much silver paint may cause the chip temperature to be higher than Nb's critical temperature, while too little paint may not provide enough adhesion. Furthermore, the very thin silver paint layer is extremely brittle at cryogenic temperatures, and the chip will desquamate from

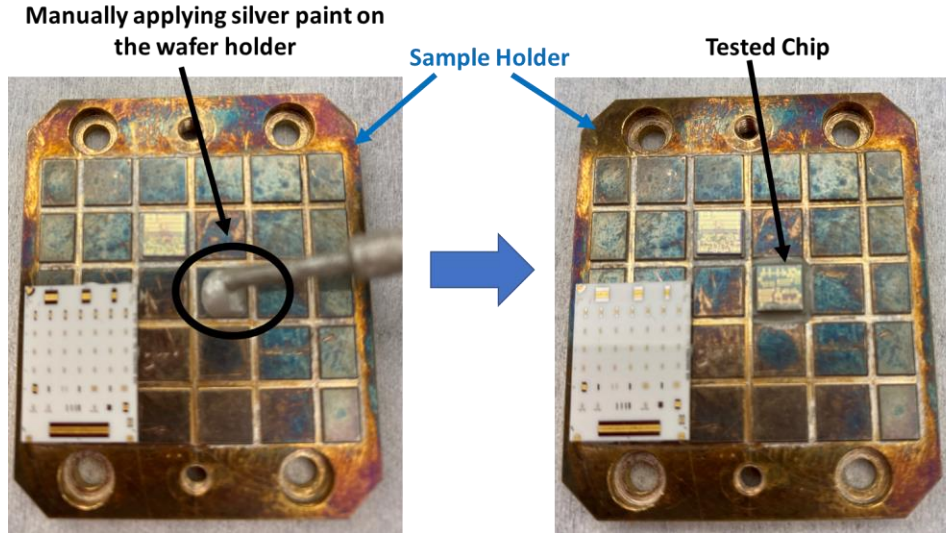


Fig. A.1 - 2. Using silver paint to mount the chip on the sample holder manually.

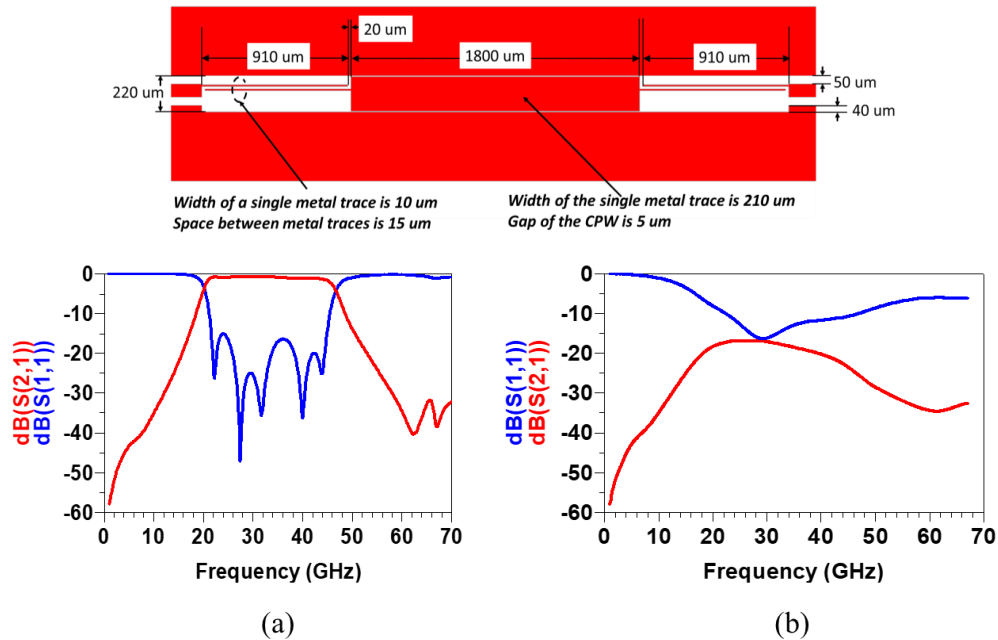


Fig. A.1 - 3. (a) The EM-simulation results of the Nb-based UWB filter assuming the conductor is lossless conductor.  
(b) The EM-simulation results of this filter assuming a finite conductivity equals to the Nb room temperature conductivity.

the wafer holder when landing the RF probes on the chip. In this section, a fabricated Nb-based UWB filter is used to demonstrate how a thick silver paint layer affects the measurement results.

Figure A.1-3 (a) shows the EM-simulation results of an Nb-based UWB filter (the MMR UWB filter shown in Chapter 5), assuming the conductor is lossless (i.e., the Nb works in the superconducting state), while Fig. A.1-3 (b) shows the EM-simulation results of this filter, assuming a finite conductivity equal to the Nb room temperature conductivity of  $6.5 \times 10^6$  S/m (i.e., the Nb works in the normal conductor state).

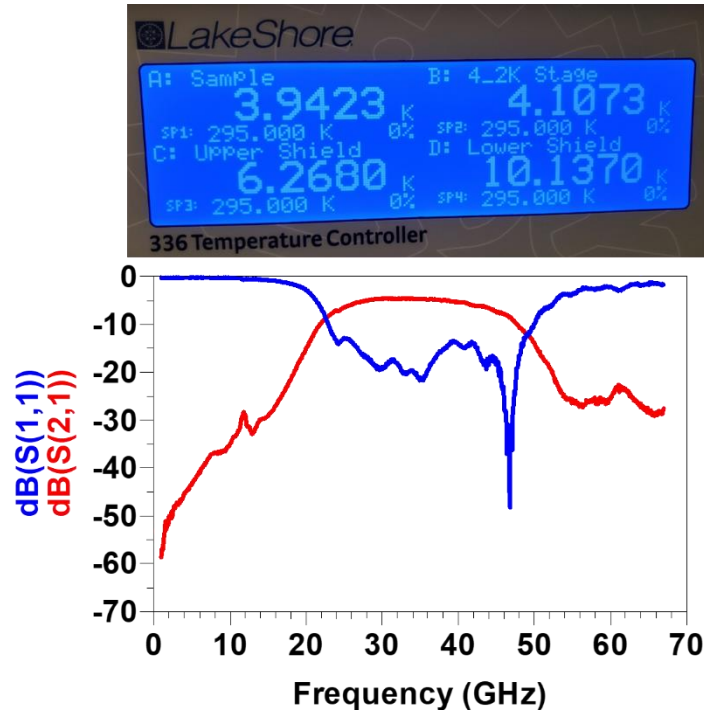


Fig. A.1 - 4. The measurement results of the fabricated Nb-based UWB filter.

Figure A.1-4 presents the measurement results for the fabricated Nb-based UWB filter. As one can see, the insertion loss is around 5dB when the Lakeshore Probe Station shows a sample stage temperature of 3.9K and a 4K shield stage temperature of 4.1k. This measured insertion loss is much higher than the EM simulation results given in Fig. A.1-3 (a). Figure A.1-5 provides measurement results for the fabricated Nb-based triple-mode UWB filter at room temperature. In comparison to the room temperature measurement results, the results shown in Fig. A.1-4 have a much lower insertion loss. From this, we can assume that some parts of the Nb in this filter have large surface resistance.

There are several possible reasons for this problem. One is that some parts of the Nb in the filter were not cooled down below Nb's critical temperature. Another possible reason is that

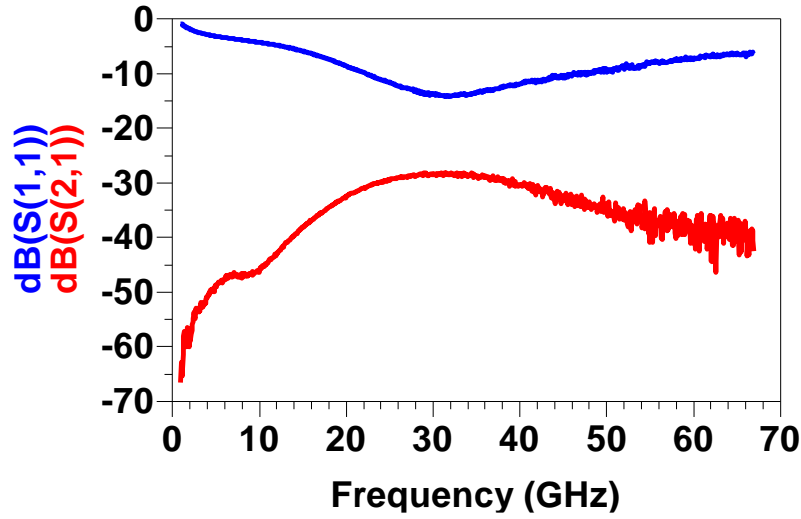


Fig. A.1 - 5. The measurement results of the fabricated Nb-based UWB at room temperature.

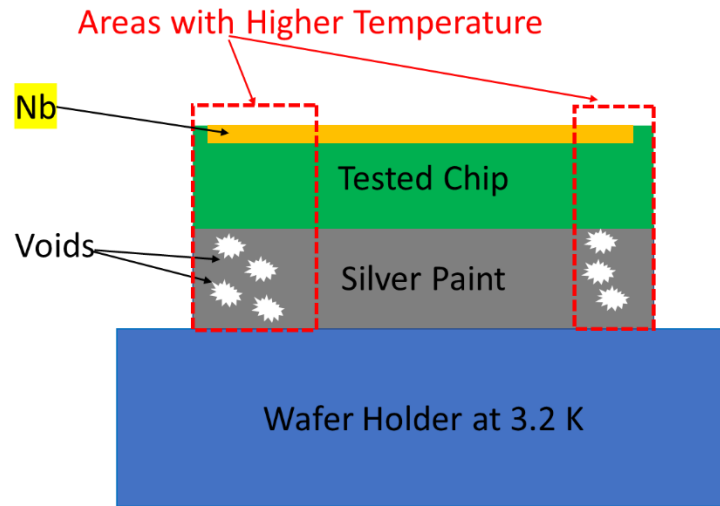


Fig. A.1 - 6. The formation of the voids in the silver paint layer leads to a local higher temperature on tested chip.

contaminations were introduced during the Nb deposition process when the filter was being fabricated. An improper calibration process can also lead to bad measurement results. By testing other RF circuits on the same tested chip (the Lange couplers presented in section 5.3), good measurement results were obtained. Thus, the reason for the higher measured insertion loss level in Fig. A.1-4 is that some parts of the Nb in this filter were not properly cooled down below Nb's critical temperature.

As shown in Fig. A.1-6, voids are formed during the post-baking process after mounting the chip on the wafer holder. The formation of voids in the silver paint layer significantly decreases the thermal conductivity of the silver paint, making parts of the Nb unable to reach critical temperature.



This problem is more pronounced when the silver paint layer is thick. Figure A.1-7 presents the measurement results of the same fabricated mm-Wave UWB triple-mode-resonator filter which was mounted on the wafer holder with a thinner silver paint layer. As one can see, the new measurement results when using a thin silver paint layer are significantly improved in comparison to the ones shown in Fig. A.1-4. For a reference, a small droplet of silver paint with a diameter of 2.5 mm is enough for mounting a 5 mm x 5 mm chip on a wafer holder (Fig. A.1-8).

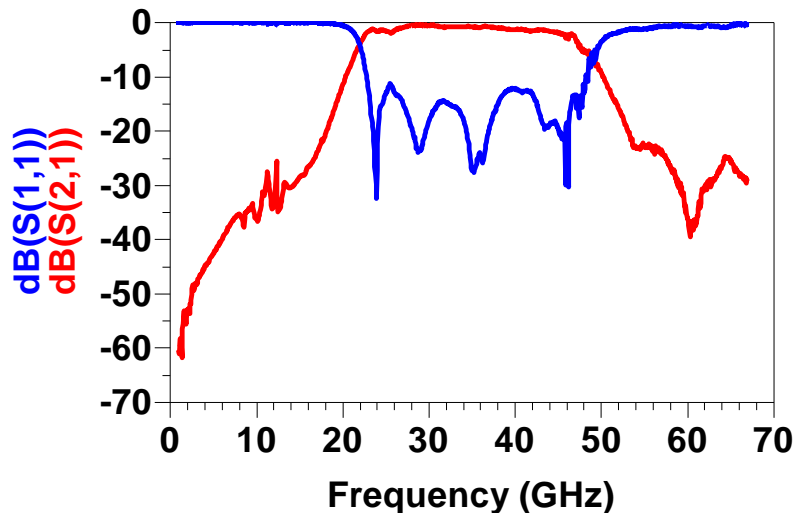


Fig. A.1 - 7. The measurement results of the fabricated UWB filter which was mounted on the wafer holder with a thinner silver paint layer.

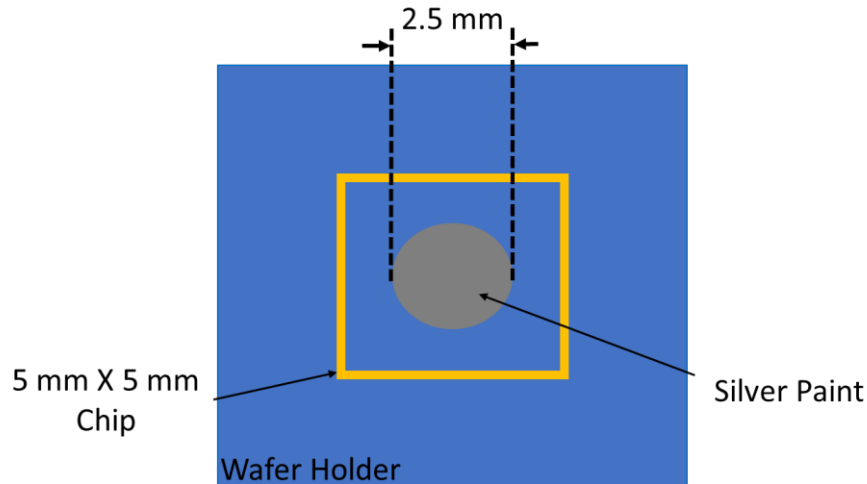


Fig. A.1 - 8. A droplet of silver paint with the diameter of 2.5 mm is enough for mounting a 5mm x 5mm chip on the wafer holder.

# Appendix B

## Micromachining Fabrication Process

This chapter will study the manufacturing process in advance and discuss the problems encountered in the preliminary experiments.

Figure B.0-1 shows a micromachine fabrication process that can be used to fabricate metallic cavity resonators on an Si wafer. First, the Si wafer is cleaned by using the standard RCA cleaning process. Then, the mask layer used for the etching process is coated and the designed patterns are transferred to the mask layer. Next, the DRIE process is used to etch the Si wafer. After the etching step, the mask layer is removed, and the metal layers are coated on the etched Si wafers.

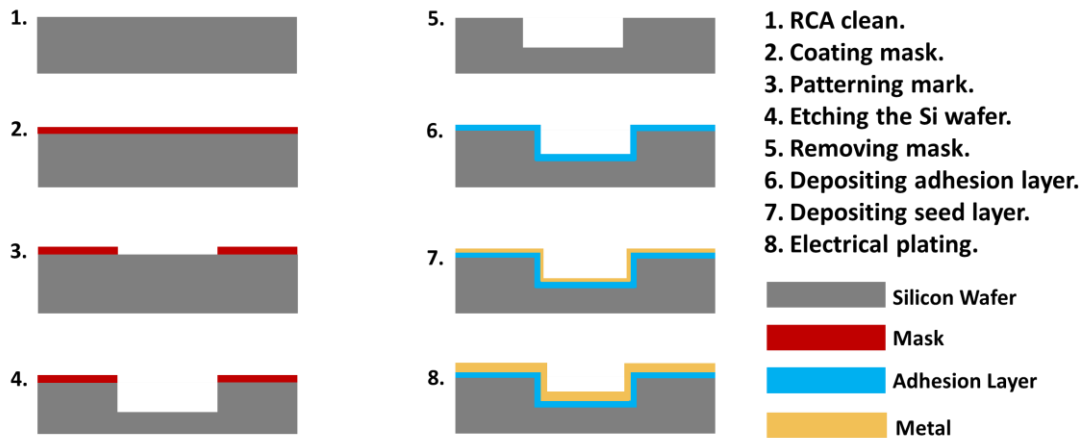


Fig. B. 0 - 1. The micromachining processes can be used to make cavities on Si wafers.

### B.1 RCA Clean

RCA clean is a standard set of wafer cleaning steps developed by Werner Kern in 1965 while working at the Radio Corporation of America (RCA). The RCA clean process ensures that no contaminants remain on the items being cleaned (in our case, Si wafers). The standard includes three steps [93]:

Step 1: Organic clean and particle clean.

Step 1 is also called RCA-1 or SC-1. The first step is performed by immersing Si wafers into a solution which is composed of Deionized (DI) water ( $H_2O$ ), hydrogen

peroxide ( $\text{H}_2\text{O}_2$ ) and ammonium hydroxide ( $\text{NH}_4\text{OH}$ ) at a ratio of 10:2:1 at 75 °C for 10 minutes. RCA-1 is used to clean organic residues and particles off the Si wafer by oxidative breakdown and dissolution. RCA-1 can also dissolve Group IB and IIB metals as well as gold, silver, copper, nickel, cadmium, zinc, and chromium.

**Step 2: Oxide strip**

The second step uses hydrofluoric acid at room temperature to remove oxide contaminations. This step is optional and is not used for the micromachining fabrication process in this chapter.

**Step 3: Ionic clean**

Step 3 is also called RCA-2 or SC-2. The step is performed by immersing the Si wafers into a solution composed of (DI) water, hydrogen peroxide ( $\text{H}_2\text{O}_2$ ) and hydrochloric acid (HCl) at a ratio of 10:2:1 at 75 °C for 10 minutes. RCA-2 is used to remove alkali ions and cations such as  $\text{Al}^{+3}$ ,  $\text{Fe}^{+3}$ , and  $\text{Mg}^{+2}$ .

## B.2 Developing a Mask Layer for DRIE

The mask layer is used to cover the area on the Si wafer that is not designed to be etched by the DRIE process. Conventionally, photoresists (PR) and  $\text{SiO}_2$  are widely used as masks for the DRIE process. Nowadays, it attracts lots of research efforts to use aluminum (Al) and Chromium (Cr) as the hard mask for the DRIE process, due to their superior etching selectivity. The etching selectivity is defined as the ratio of the thickness of the Si etched versus the thickness of the mask consumed during the etching process. Table B.1 summarizes a comparison of using different materials as a mask for the DRIE process [94]-[95].

Table B.1 Comparison of using different materials as the mask for the DRIE process.				
Mask Material	Typical Selectivity to Si	Critical Dimensions	Mask Development	Micro-masking Problems During DRIE Process
PR	< 100	Moderate	Simple/Fast	No
$\text{SiO}_2$	100 - 300	Fine	Complex/Slow	No
Al	$\sim 10^5$	Very Fine	Complex/Slow	Yes

### B.2.1 Using Aluminum as DRIE Hard Mask

Aluminum has the superior selectivity of  $10^5:1$ , and thus an aluminum mask layer is extremely thin. With such a thin mask layer, very high aspect ratio structures with a submicron critical dimension can be etched with high accuracy. However, there are still challenges when using aluminum as a hard mask. The first well-known challenge is the formation of micro-masking. During the etching process, accelerated ions bombard the mask layers. Mask particles will be generated and randomly re-deposit on the wafer. If the mask particles are deposited in the designed etching area, the designed structures will be destroyed. This problem is more pronounced in long-duration etching processes to achieve a deep structure. Micro-masking problems can easily be solved by tuning the bias power or temperature when using photoresist and  $\text{SiO}_2$  as masks [96]. However, micro-masking problems are difficult to solve when using aluminum as the hard mask.

The second challenge is that aluminum particles randomly generated from the mask layer will be accelerated and can bombard and break the passivation layers on the sidewalls, as shown in Fig. B.2-1. Although some publications reported the potential solutions for those problems [94] and [97], there is still no mature means to overcome those challenges of using aluminum as a hard mask for long-duration DRIE processes.

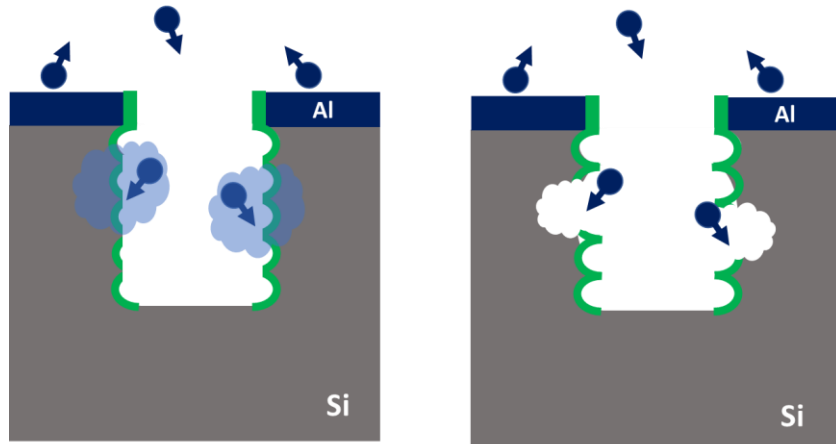


Fig. B. 2 - 1. The accelerated aluminum atoms can destroy passivation layers on the sidewall. [94]

### B.2.2 Using $\text{SiO}_2$ as DRIE Hard Mask

To use  $\text{SiO}_2$  as a mask for the DRIE process,  $\text{SiO}_2$  needs to be coated on the Si wafers first. The  $\text{SiO}_2$  layer can be deposited on the wafers by using plasma-enhanced chemical vapor deposition

(PECVD) or RF sputtering. However, depositing an SiO<sub>2</sub> layer several microns thick for the long-duration DRIE process takes several hours. The thermal oxidation method can handle 50 - 100 Si wafers simultaneously, but an extra polishing step is required to remove the SiO<sub>2</sub> from the backside of the Si wafer.

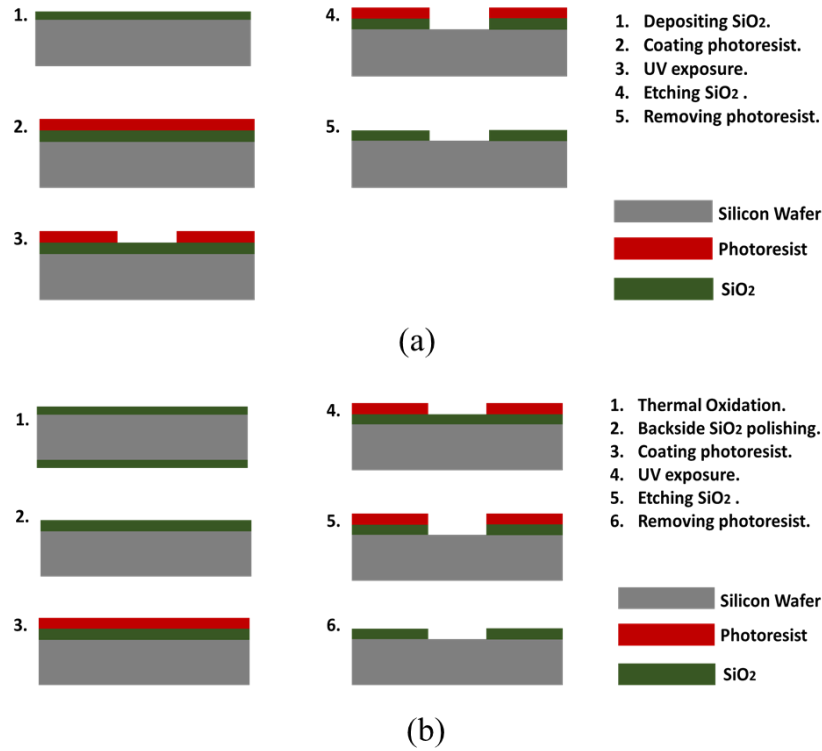


Fig. B. 2 - 2. (a) The steps to develop the SiO<sub>2</sub> mask layers for DRIE process with using the PECVE (or RF Sputtering) to deposit SiO<sub>2</sub> on the Si wafer. (b) the steps to develop the SiO<sub>2</sub> mask layers for DRIE process with using the thermal oxidation to coat to SiO<sub>2</sub> on the Si wafer.

Figure B.2-2 shows the steps for developing SiO<sub>2</sub> mask layers for the DRIE process using PECVE (or RF sputtering) and thermal oxidation to coat the SiO<sub>2</sub> on the Si wafers. After successfully coating the SiO<sub>2</sub> layer on the Si wafer, the SiO<sub>2</sub> layer needs to be etched with the designed patterns. Etching SiO<sub>2</sub> can be done by using either a wet etching technique or a dry etching technique. Wet etching SiO<sub>2</sub> requires the use of lethal toxic hydrofluoric acid (HF). Although wet etching thick SiO<sub>2</sub> with HF can provide a high etching speed, the aggressive chemical reactions may lead to a highly isotropic etched structure, and it is very difficult to control the etching direction. SiO<sub>2</sub> can also be etched an-isotropically by using RIE technology. In this case, however, a thick photoresist layer is necessary as the mask layer for the SiO<sub>2</sub> etching process. Furthermore, it takes a much longer time to etch through several micrometers of SiO<sub>2</sub> using RIE. For example, it could take several hours to etch through a 4 μm thick SiO<sub>2</sub> layer by using the PlasmaPro 100 Cobra® ICP Etch system with C<sub>4</sub>F<sub>8</sub> as the etching gas. Moreover, the etching product of the SiO<sub>2</sub> RIE process

forms a thin residual layer in the processing chamber. This requires the following oxygen plasma cleaning process to be run for at least the same length of time as the SiO<sub>2</sub> etching process.

Although it is time-consuming to coat and etch SiO<sub>2</sub>, using SiO<sub>2</sub> as a hard mask for DRIE has some advantages compared to using aluminum and photoresist. The use of SiO<sub>2</sub> as a hard mask for DRIE does not have the micromasking problems associated with the use of aluminum. Further, SiO<sub>2</sub> has better selectivity than the photoresist. SiO<sub>2</sub> coated on an Si wafer using the thermal oxidation method can have a selectivity of 300, as SiO<sub>2</sub> has better thermal and chemical stability during the DRIE process than the photoresist. Moreover, for the micromachine metallic cavity filters, there is no need to remove the SiO<sub>2</sub> mask layer after the DRIE process and the conductor layers can be directly coated on the SiO<sub>2</sub> layer.

### B.2.3 Using Photoresist as DRIE Mask

To coat the photoresist on the wafer, a few milliliters of photoresist are dispensed on the wafer first, as shown in Fig. B.2-3. Then, the wafer is brought to a rotational speed of several thousand revolutions per minute (rpm). As the wafer is rotating, the centrifugal force makes the dispensed resist spread uniformly across the wafer, as depicted in Fig. B.2-3. The thickness of the coated photoresist depends on the wafer's rotational speed. The higher the rotational speed, the thinner the photoresist film. Typically, the wafer needs to be rotated for around 10 to 30 seconds, and the entire photoresist coating time is normally less than one minute.

Due to the low selectivity of photoresists, a thick photoresist mask layer is necessary for the long-duration DRIE process to achieve a deep structure. The most common problem when using a thick photoresist coating is the formation of edge beads, as illustrated in Fig. B.2-4. When the wafer is rotating at high speed, the air turbulence above the edge of the wafer causes the photoresist at the wafer edge to dry off faster. This will suppress the extra photoresist from spinning off from the wafer and make excessive photoresist accumulate at the wafer edge. Figure B.2-5 presents a photo of a

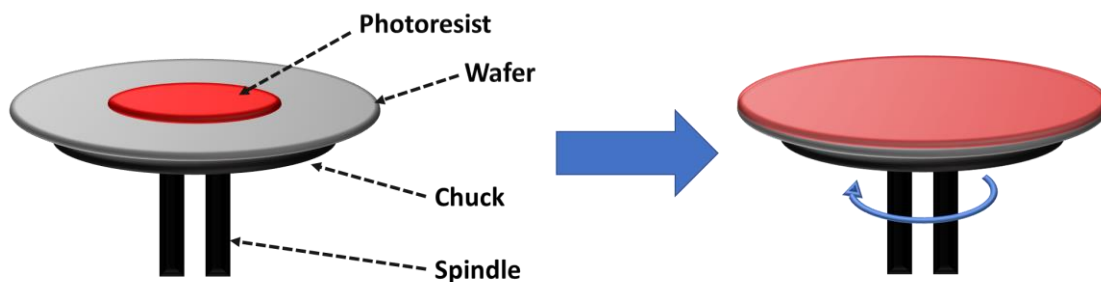


Fig. B. 2 - 3. Coating photoresist on wafers by using the spring coater. [99]

4-inch Si wafer coated with 17  $\mu\text{m}$  thick positive photoresist, AZ® P4620 [98]. As shown, the photoresist layer is much thicker at the wafer's edge.

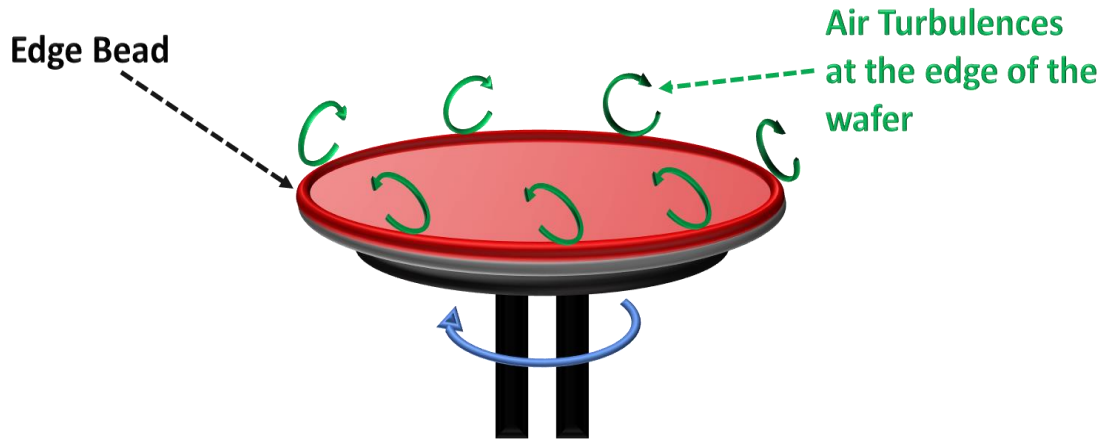


Fig. B. 2 - 4. The formation of edge bead when using thick photoresist. [100]

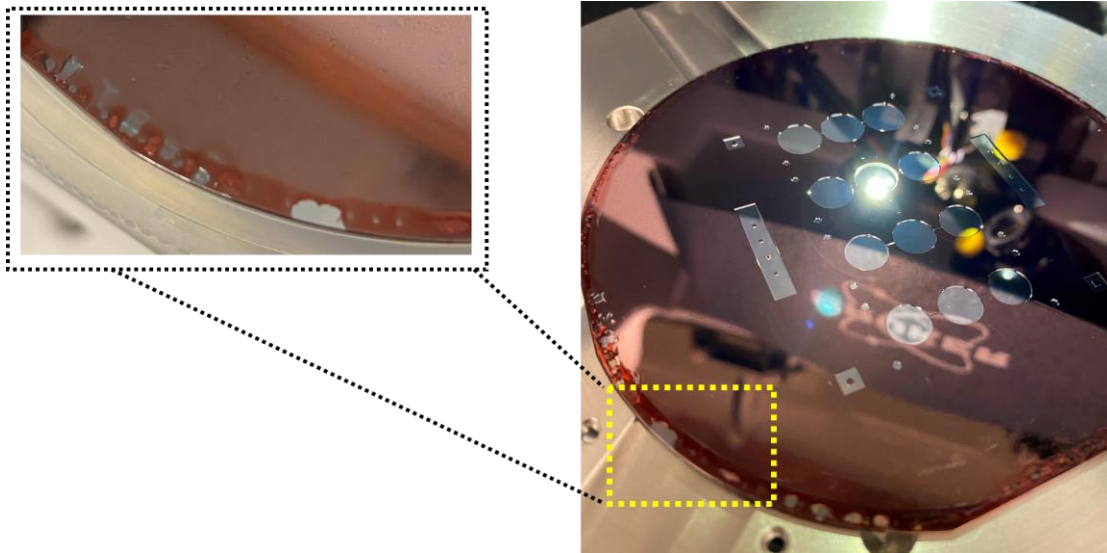


Fig. B. 2 - 5. The photo of a 4-inch Si wafer coated with 17  $\mu\text{m}$  thick positive photoresist, and the portions of the edge bead come off the Si wafer during the DRIE process.

Moreover, edge beading can be destructive for the subsequent micromachine process steps. As shown in Fig. B.2-6, an edge bead introduces an unexpected space between the photoresist film and the patterned UV mask. This can lead to poor resolution and wrong dimensions for the UV exposure step. Moreover, there will be a significant amount of residual solvent content in the thick edge bead after the soft-bake process. Thus, the patterned UV mask may stick to the Si wafer after the contact UV exposure.

Also, as depicted in Fig. B.2-7, clamps are used to press the wafer at the edge and hold the wafer tightly on the chamber table during the DRIE process. The high temperature plasma can melt the thick edge bead. This can make the Si wafer stick to the clamps and get stuck in the DRIE processing chamber. The photo in Fig. B.2-5 illustrates how portions of edge bead photoresist were chipped off from a Si wafer and remained on the clamps after the DIRE process chamber.

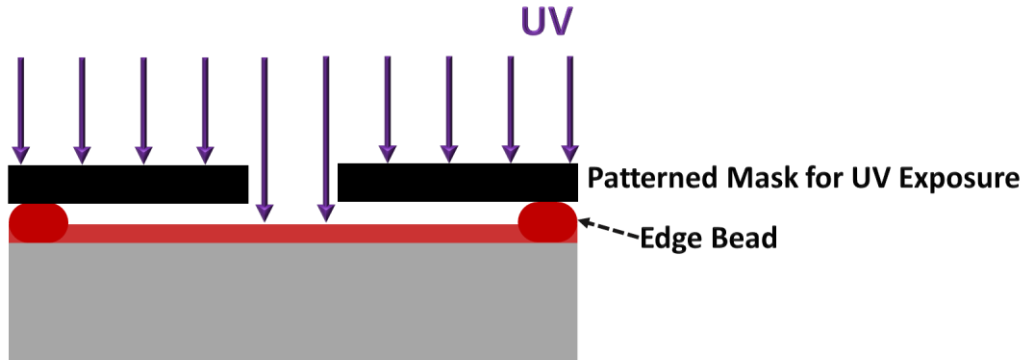


Fig. B. 2 - 6. The edge bead introduces the unexpected space between the photoresist film and the patterned UV mask.

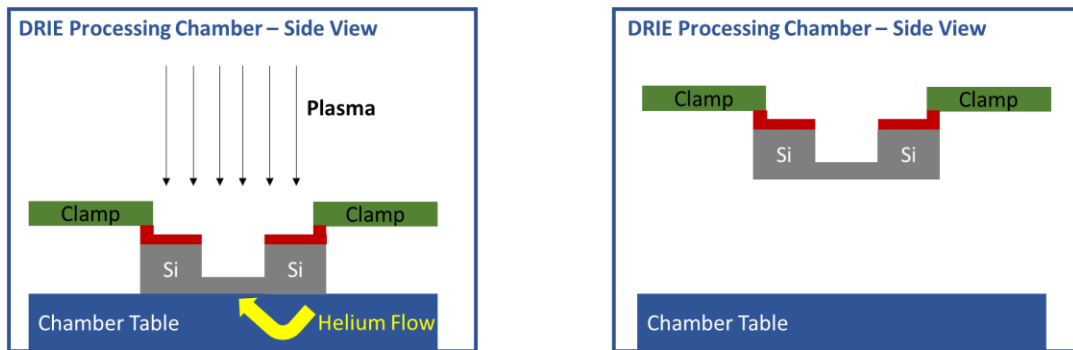


Fig. B. 2 - 7. With a thick edge bead, the Si wafer will stick on the clamp in the DRIE process chamber. [101]

To remove the edge bead, the Brewer Cee® 200X Precision Spin Coater at the Quantum-Nano Fabrication and Characterization Facility (QNFCF), University of Waterloo, was used. This spin coater has a fine nozzle (Fig. B.2-8), which is employed for rinsing the wafer's edge with solvent (AZ® EBR) while the wafer is rotating. Figure B.2-9 shows a photo of a 4-inch Si wafer coated with 17  $\mu\text{m}$  thick positive photoresist (AZ® P4620) with the edge bead removed.

After coating the PR masker layer on the Si substrate, a soft-bake is required to reduce the residual solvent concentration in the photoresist film and to improve the photoresist adhesion to the Si wafer. For a 17  $\mu\text{m}$  thick AZ® P4620 film, the soft-bake is done by baking the coated Si wafer with a hotplate at 110°C for 3 minutes. The UV exposure step is done by using a Heidelberg



MLA150 Maskless Aligner with a laser (405 nm wavelength) energy density of  $800 \text{ mJ/cm}^2$  at the QNFCF (University of Waterloo). After the UV exposure process, the Si wafer was immersed in the developer (AZ® 400K) at room temperature for 5 minutes and then rinsed with deionized water (DI water) for 1 minute. Finally, the wafer is blown dry with nitrogen. Figure B.2-10 presents photos of the photoresist development setup and a developed photoresist coated Si-wafer with the designed patterns.

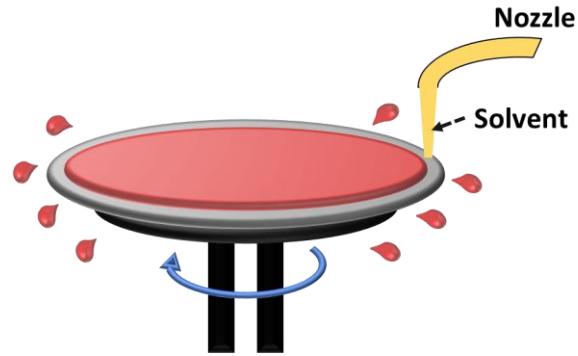


Fig. B. 2 - 8. The schematic shows how the edge beam is removed by using the Brewer Cee® 200X Precision Spin Coater. [102]

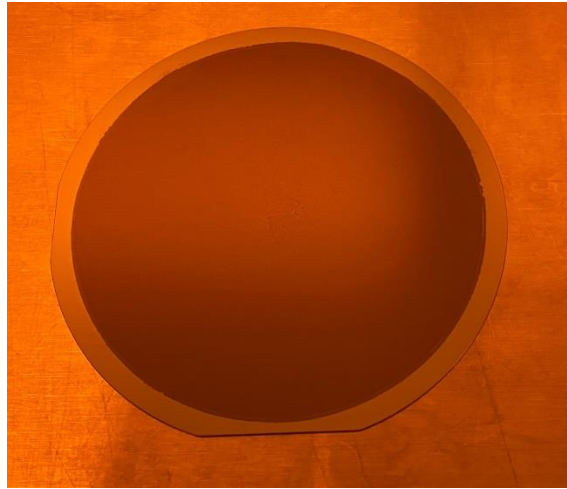


Fig. B. 2 - 9. The photo of a 4-inch Si wafer coated with  $17 \mu\text{m}$  thick positive photoresist and the edge bead is removed.

After developing the photoresist layer, there is a significant amount of residual solvent in the thick photoresist layer. Moreover, as shown in Fig. B.2-11, the solvent concentration is higher at the bottom portion of the thick photoresist layer than at the top portion of the thick photoresist layer. The hard-baking step helps any residual solvent evaporate from the thick photoresist layer. Furthermore, this step is necessary to improve the thermal and chemical stability of the photoresist,

especially when the thick photoresist layer is used as a mask for the subsequent plasma etching process (e.g., Si or SiO<sub>2</sub> etching).

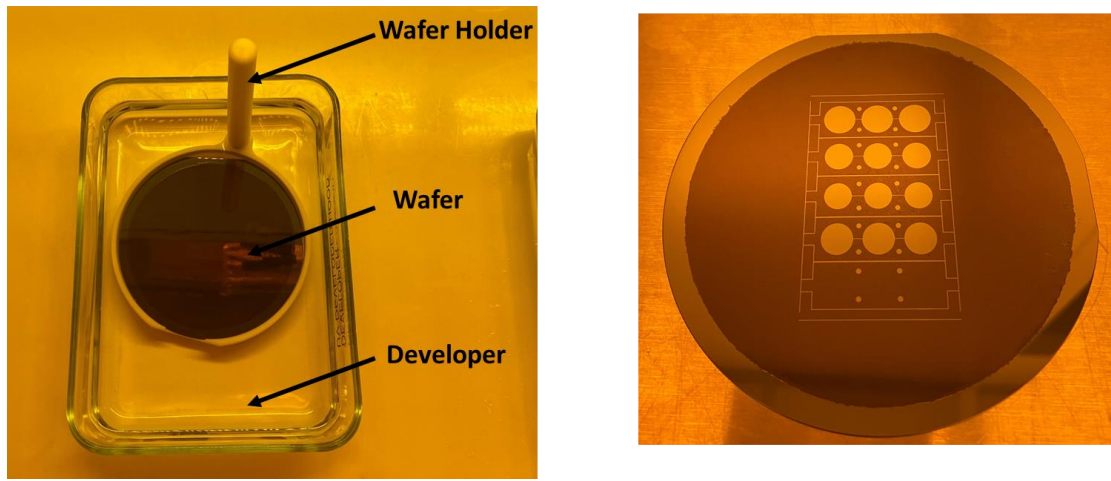


Fig. B. 2 - 10. The photos of the photoresist development setup and a developed photoresist coated Si-wafer.

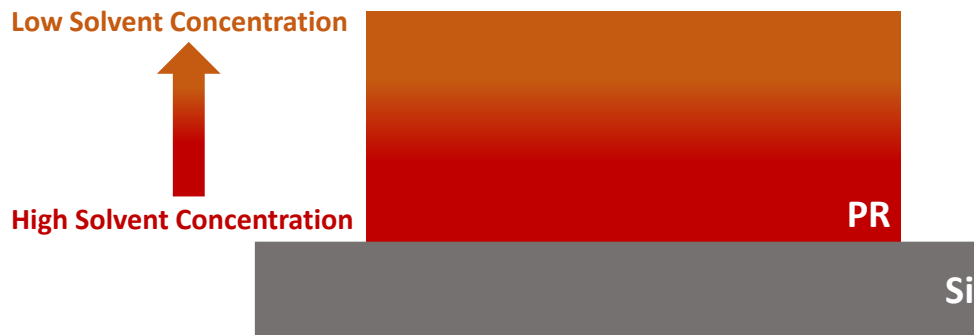


Fig. B. 2 - 11. The solvent concentration in the photoresist layer.

The hard-bake can be done by using an oven or hotplate. As depicted in Fig. B.2-12, an oven applies heat to the photoresist-coated wafer from all directions via the air, while a hotplate applies heat to the wafer from the bottom via a flat metallic plate. Therefore, by using a hot plate, the time it takes for the photoresist to reach the target temperature is much shorter. Another potential problem with using an oven is that after opening and loading the oven, the temperature-hysteresis during the heating process may cause the temperature of the photoresist to greatly exceed the target temperature. As depicted in Fig. B.2-13, heat is applied to the photoresist from all directions in an oven and a hard photoresist shell (shown in black) may form when the hard-bake is done. This hard photoresist shell locks most of the residual photoresist solvent molecules (shown in blue) inside, which could cause severe problems during the subsequent Si plasma etching process.

As an example, Fig. B.2-14 (a) presents a photo of an Si wafer etched by using the DRIE process for 12 minutes. This Si wafer was baked in a cleanroom oven at 85°C for 50 minutes after the photoresist development step. As one can see, the photoresist maintains relatively good shape. Figure B.2.14 (b) shows a photo of the same Si wafer etched by the same DRIE process for an extra 12 minutes. As can be seen, the photoresist surface becomes foam-like after the second etching. During the second 12-minute etching round, a hard shell that formed in the conventional oven was etched out, and the photoresist with high solvent concentration was exposed in the high temperature plasma and started bubbling. The bubbles destroyed the images on the patterned photoresist mask.

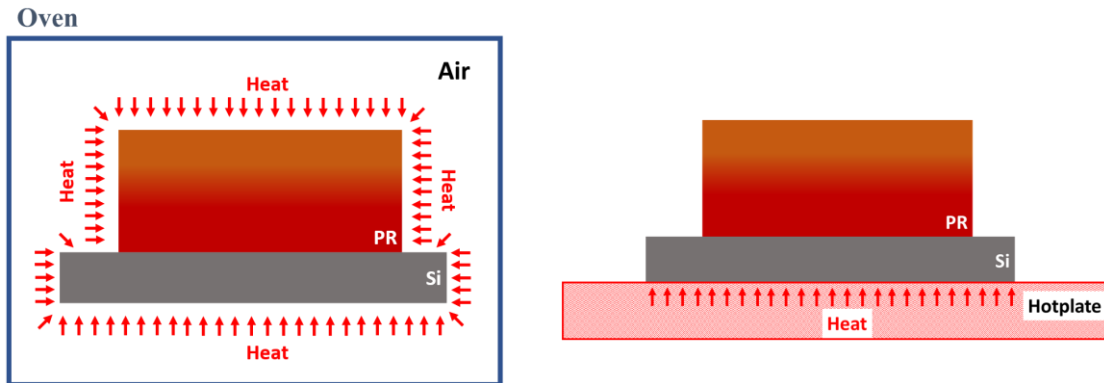


Fig. B. 2 - 12. Baking the wafer by using the oven and the hotplate.

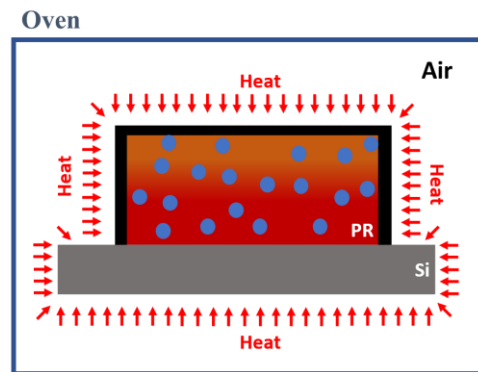
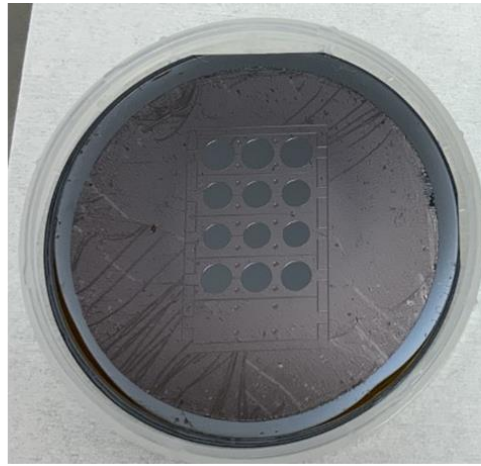


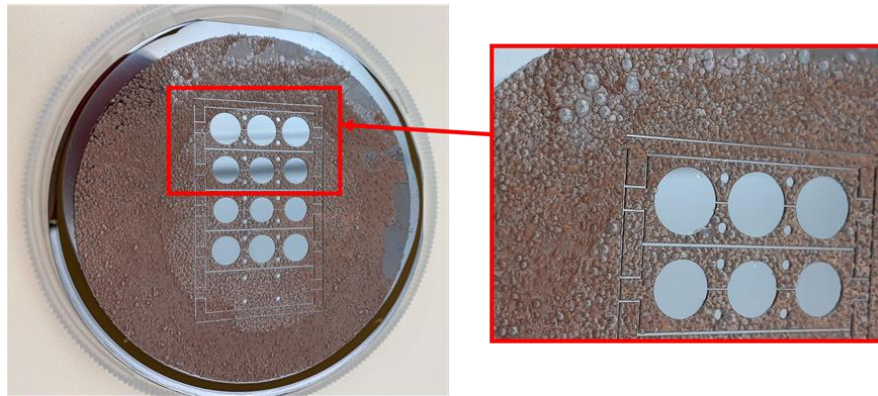
Fig. B. 2 - 13. The outer layer of the photoresist may form a hard shell when the wafer is baked in an oven.

When using a hotplate to do the hard-baking, the heat is applied from the bottom of the wafer, as depicted in Fig. B.2-15. The photoresist solvent molecules can easily evaporate from the top. The hard-bake efficiency can be further improved by increasing the air flow on top of the photoresist. Figure B.2-16 shows a photo of an Si wafer with a 17  $\mu\text{m}$  thick AZ® P4620 layer etched by using the DRIE process for three 12-minute rounds, using the same recipe as the wafer shown in Fig.

B.2-14. Before the DRIE process, this wafer was hard-baked by using a hotplate at 115°C for 15 minutes. As can be seen, the photoresist remains in good shape after the DRIE process.



(a)



(b)

Fig. B. 2 - 14. (a) the photo of a Si wafer etched by using the DRIE process for 12 minutes. (b) shows the photo of this Si wafer was etched by the same DRIE process for an extra 12-minutes etching round.

It should be mentioned here that the baking temperature and duration should be optimized depending on the photoresist material, the photoresist thickness, the design patterns, and the subsequent micromachine fabrication processes. In addition, the subsequent plasma etching process should be performed immediately after the hard-baking step. This is because the thick photoresist can absorb water molecules from the air, thereby rehydrating the thick photoresist. If the plasma etching process cannot be performed after the hard-baking step, an additional hard-baking step is required prior to the plasma etching process.

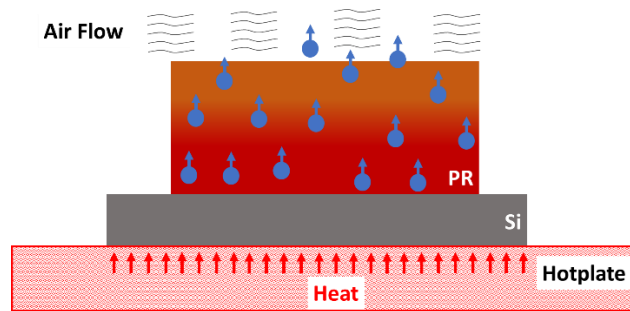


Fig. B. 2 - 15. The photoresist solvent molecules can easily evaporate from the top when the wafer is baked on a hotplate.

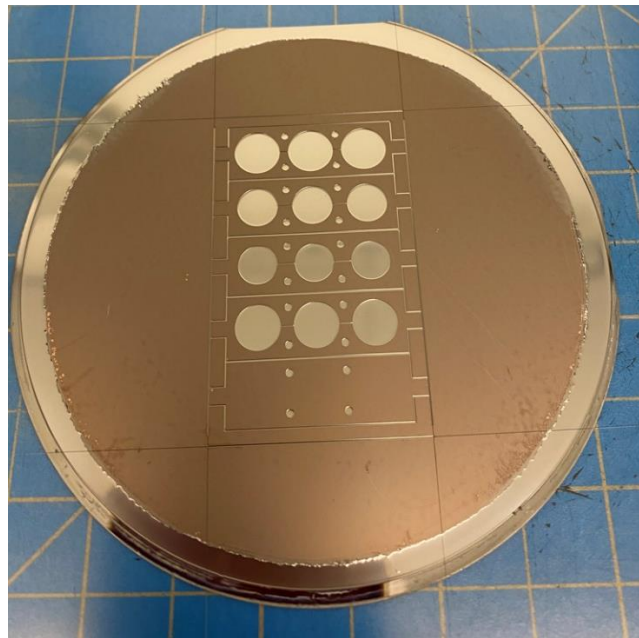


Fig. B. 2 - 16. A Si wafer was baked on a hotplate at 115°C for 6 minutes, and then etched by using DRIE process for 36 minutes.

### B.3 Etching Si Wafers Using DRIE

The Si etching processes were done using the PlasmaPro 100 Cobra® ICP Etch system at the Centre of Integrated RF Engineering located in the University of Waterloo. Figure B.3-1 depicts a schematic of the PlasmaPro 100 Cobra® ICP Etch system. Passivation and etching gases are injected into the vacuum processing chamber from the top, while an inductively-coupled plasma (ICP) generator is used to generate the plasma. A vacuum pump is connected to the bottom of the processing chamber and used to control the pressures and vacuum the etching products out of the processing chamber. A separate RF generator connected to the chamber table is used to provide the

bias voltage that accelerates the ions. The chamber table is cooled down, and the helium flow can be injected between the chamber table and the wafer to improve the thermal conductivity. Thus, the wafer temperature remains at low temperature during the DRIE process.

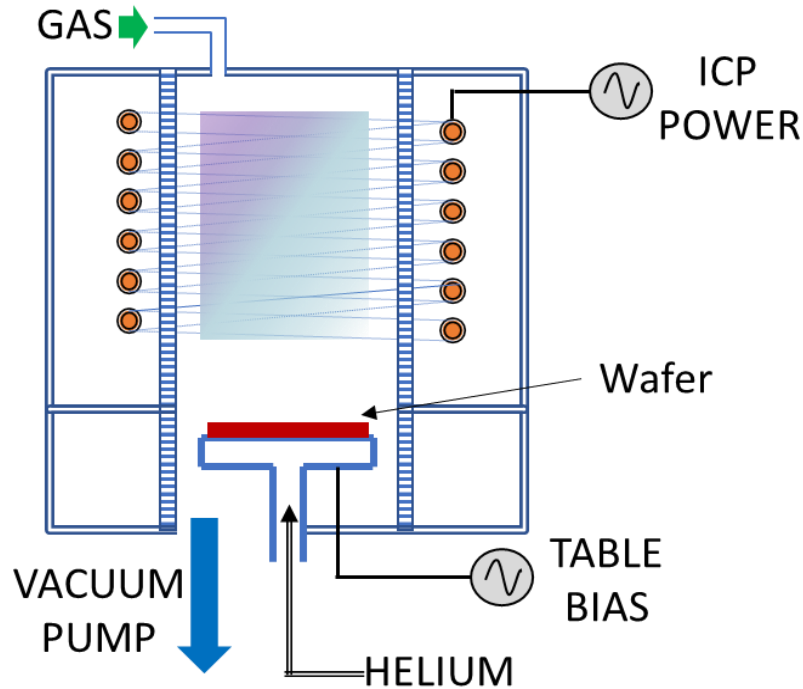


Fig. B. 3 - 1. The schematic of a PlasmaPro 100 Cobra® ICP Etch system. [101]

As described in Chapter 2, the Bosch DRIE process works by simply alternately repeating the passivation and etching steps. However, the performance of this process is controlled by twelve parameters, as listed below:

- 1) Passivation gas flow.
- 2) Passivation step time.
- 3) ICP power level for the passivation step.
- 4) Bias power lever for the passivation step.
- 5) Chamber pressure for the passivation step.
- 6) Etching gas flow.
- 7) Etching step time.
- 8) ICP power level for the etching step
- 9) Bias power lever for the etching step.
- 10) Chamber pressure for the passivation step.

- 11) Wafer table temperature.
- 12) Helium flow rate.

All of these parameters will affect the etching performance [20] - [22]. Adjusting twelve parameters is an arduous and time-consuming process, but some general guidelines can be followed to help the parameter adjustment process. The gas flow rate, the ICP power level, and the chamber pressure control the particle and ion densities in the plasma. A higher particle and ion density in the passivation gas plasma results in the formation of a thicker passivation layer. A higher particle and ion density in the etching gas plasma results in a higher Si etching rate, but reduces the etching selectivity of the mask. A higher bias power level during the etching step leads to a higher etching rate, but the etching selectivity between the Si and the mask is lower. The passivation step time and the etching step time affect the surface roughness of the structure sidewalls and the etching rate. The wafer table temperature and the helium flow rate control the temperature on the wafer. A high wafer temperature leads to a low etching selectivity between the Si and the mask. Note that all of these parameters need to be adjusted for different design structures.

In addition to the above parameters, the designed geometric pattern will also affect the performance of the DRIE process. Under the same process parameter settings, the etching rate of a design pattern with a larger aspect ratio is higher than that of a design pattern with a smaller aspect ratio. This is known as aspect ratio-dependent etching (ARDE). Figure B.3-2 presents a photo of an Si piece etched through by using the DRIE process. As can be seen, the large circuits (with diameters larger than 5 mm) were completely etched through, while the 150  $\mu\text{m}$  wide trenches between the three bigger circuits was not. Thus, when using DRIE to etch through the Si wafer, it is important to calculate the required processing time based on the minimum feature size of the design pattern.

The etching rate of the DRIE process is not constant. As the depth of the etched area increases, it becomes more difficult for the etching gas and etching products to reach and exist from the bottom of the etched area. Thus, the etching rate decreases as the depth of the etched area increases. This problem is particularly prominent for a long-duration etching process to achieve a structure with a depth of several hundred microns. Therefore, in order to obtain accurate long-duration etching rate characteristics, it is necessary to perform multiple long-duration etching tests.

Ideally, the plasma should be evenly distributed over the entire wafer. However, the area near the center of the wafer has a higher plasma density than the area near the wafer's edge. Therefore, the design patterns close to the center experience a higher etching rate than the patterns close to the



edge. Moreover, as shown in Fig. B.3-3, the design patterns in the blue box have a slower etching rate than the design patterns in the red box. The local plasma density of the dense etching pattern in the blue frame is lower than that of the scattered etching pattern in the red frame. To solve this problem, the Si wafer can be diced into small silicon pieces. By mounting them in the center of a carrier wafer, an additional DRIE process can be applied to those Si pieces with slower etching rates than in the previous DRIE process.

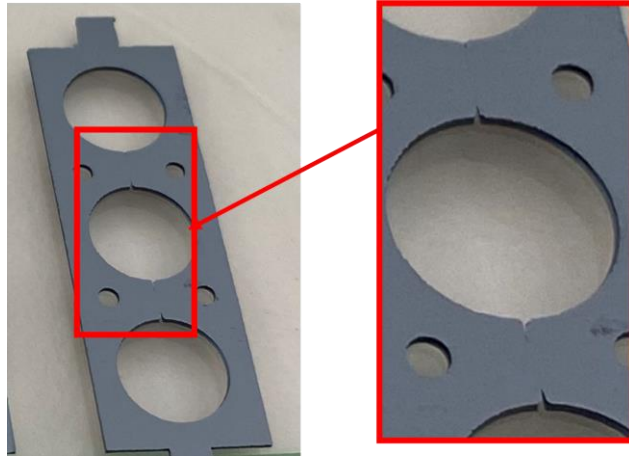


Fig. B. 3 - 2. The design patterns with a larger aspect ratio were etched through, whilst the design patterns with a smaller aspect ratio were not fully etched through.

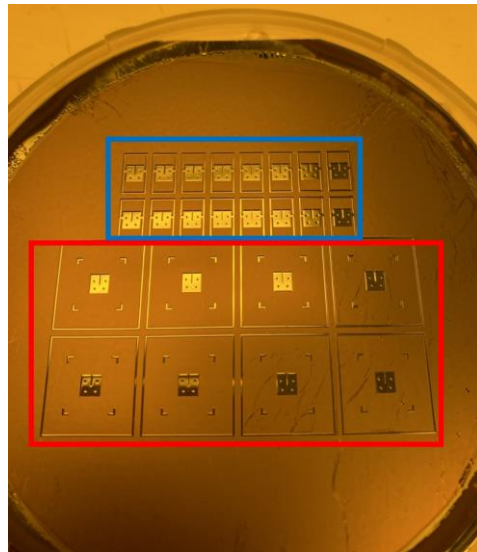


Fig. B. 3 - 3. The density of the etching pattern distribution on the silicon wafer can affect the etching rate.



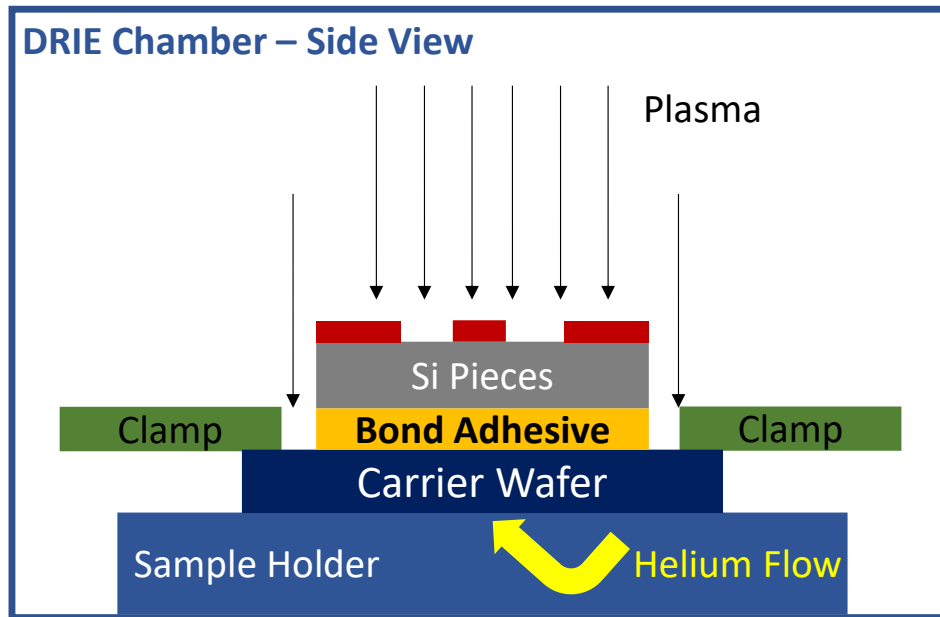


Fig. B. 3 - 4. The small Si piece is bonded on the carrier wafer by using bonding adhesives.

When using a carrier wafer, the small Si piece needs to be bonded on the wafer by using bonding adhesives, as shown in Fig. B.3-4. Vacuum pump fluid and crystal-bond wax are two of the most common bonding adhesives. One of the major differences between these two bonding adhesives is that the vacuum pump fluid has a good thermal resistance, whereas the crystal-bond wax has reasonably good thermal conductivity. When using the photoresist as a mask layer for the DRIE process, crystal-bond wax is a better choice, since the etching selectivity of the photoresist is very sensitive to the wafer temperature. For example, when all other etching parameters are the same, the etching selectivity of the photoresist is about 100 at 0°C, while the etching selectivity of the photoresist drops to 70 at 15°C. When vacuum pump fluid is used, heat conduction between the Si piece and the carrier wafer is inhibited. This leads to a high processing temperature on the Si piece, and the etching selectivity of the photoresist can drop below 10. In this case, the photoresist mask layer will be used up before the expected etching depth is reached, and the non-flat thick photoresist surface will be transferred to the final etched Si pieces. For example, as shown in Fig. B.3-5, the surfaces of the etched-through Si pieces are rough and the thickness of the Si pieces is only 430  $\mu\text{m}$ .

Due to the working principle of the Bosch DRIE process, scalloping sidewall surfaces are inevitably formed. Although the smoothness of the sidewall surface can be improved to a certain extent by adjusting the etching parameters, for applications that require extreme smoothness, additional steps are necessary. Figure B.3-6 shows a way to improve sidewall surface smoothness, which was demonstrated by nanoFab Fabrication and Characterization Centre at University of

Alberta. After the DRIE process, the mask and passivation layers are removed first. Then, the Si wafer is oxidated to grow a thin  $\text{SiO}_2$  film on the surface. Finally, the  $\text{SiO}_2$  etching technology can be used to remove the thin  $\text{SiO}_2$  film. [103]

The thick photoresist mask layer is hardened during the DRIE process. Normally, it takes several hours to completely remove a thick photoresist mask layer by soaking the wafer in photoresist

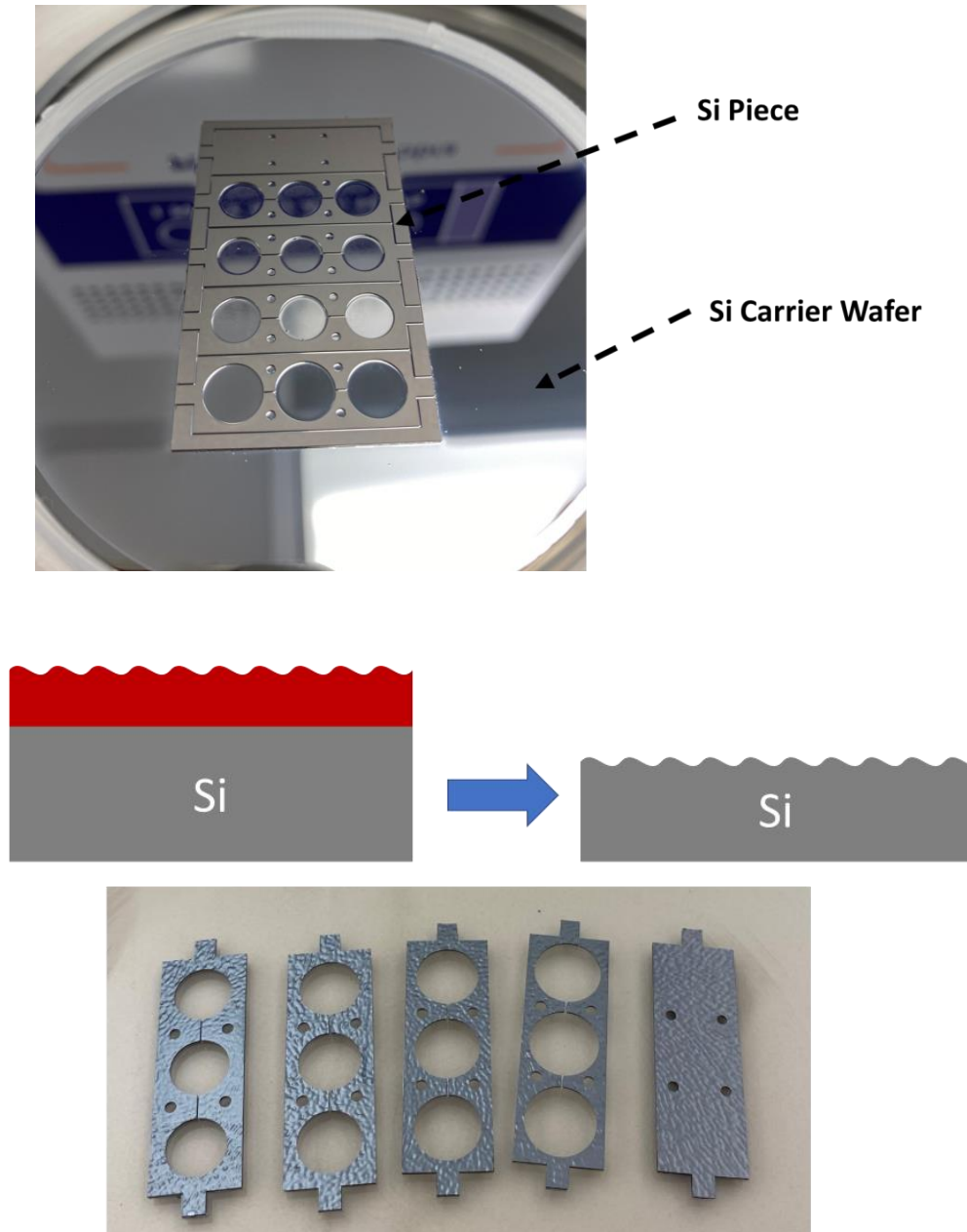


Fig. B. 3 - 5. The Si piece is bounded on the carrier wafer by using the vacuum pump fluid as the adhesive. The photoresist mask was used up before reaching the expected etching depth, and the non-flat thick photoresist surface were transferred to the final etched Si pieces.

stripper solvents. Two methods can be used to remove a thick photoresist mask layer more efficiently.

The first method is soaking the wafer in Remover PG (70°C) in combination with ultrasonics. Under normal conditions, a thick photoresist mask layer can be totally removed with a low ultrasonic power level after 20 minutes. Figure B.3-7 shows the setup of this cleaning method. If a cross-link between the photoresist and Si is formed during the plasma etching process, a high ultrasonic power level can be used to clean the residual photoresist. The major drawback of this method is that the mechanical structures of the Si pieces can be damaged by high ultrasonic power, as shown in Fig. B.3-8.

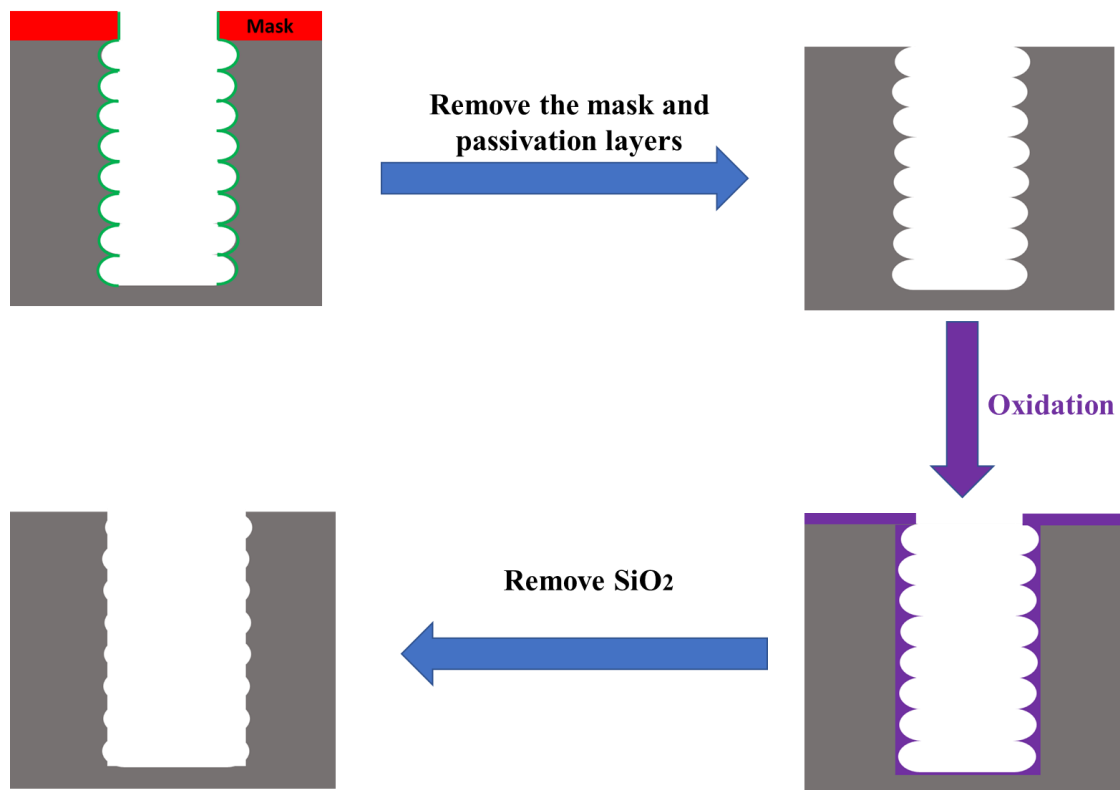


Fig. B. 3 - 6. A possible way to to improve sidewall smoothness after the DRIE process. [103]

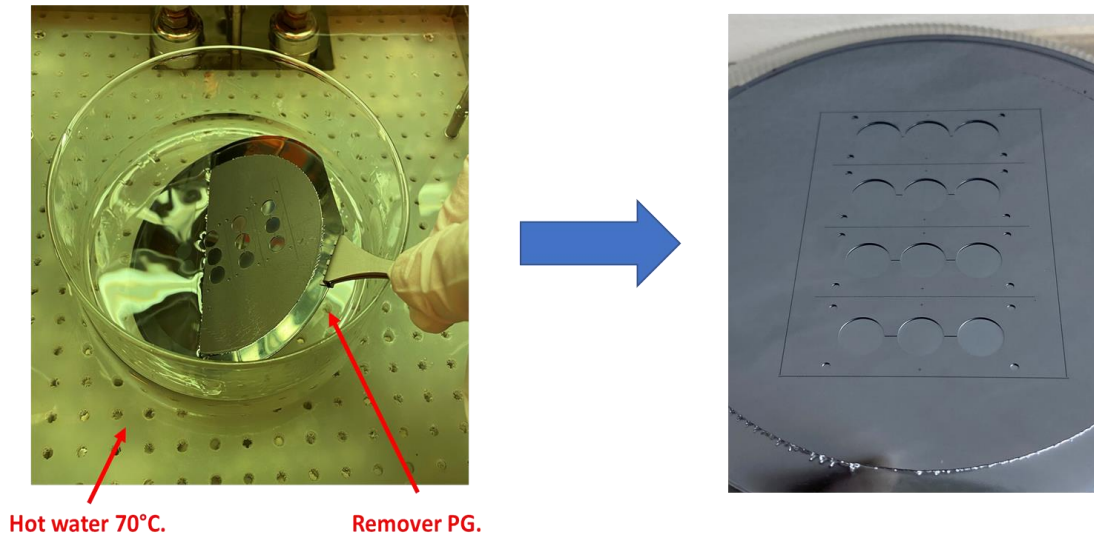


Fig. B.3 - 7. Using Remover PG combining ultrasonic to strip the mask layer after the DRIE process.



Fig. B.3 - 8. The mechanical structure of the Si piece was damaged by the high ultrasonic power.

The second method is cleaning the wafer by using a piranha solution. This method can remove organic residues from a substrate very efficiently. The drawback of this method is that the piranha cleaning process is very dangerous and toxic, since the solution is made by mixing sulfuric acid ( $\text{H}_2\text{SO}_4$ ) and hydrogen peroxide ( $\text{H}_2\text{O}_2$ ). If the piranha process is necessary, the operator must be well-trained, and the piranha cleaning process should be done at a specified wet bench.

## B.4 Coating the Metal Layer

After the DRIE process, the metal layers need to be coated on the etched Si wafers (or Si pieces). The metal plating experiments were done by using the Intlvac® Nanochrome Deposition System at CIRFE (University of Waterloo). This metal deposition system has two functions: a metal sputtering deposition function (Fig. B.4-1) and an e-beam evaporation deposition function (Fig. B.4-2). The metal sputtering deposition function uses high-speed argon particles to physically bombard the sputtering target and generate metal particles. The metal particles are then deposited on the Si wafer. The e-beam evaporation deposition function uses a high-temperature electron beam to irradiate the metal target, so that the evaporated metal forms a thin film on the Si wafer. Since the metal particles produced by the metal sputtering deposition function have more kinetic energy, the sidewalls of the etched structures on the Si wafer can be covered with metal well, while e-beam evaporation deposition function cannot provide good sidewall coverage.

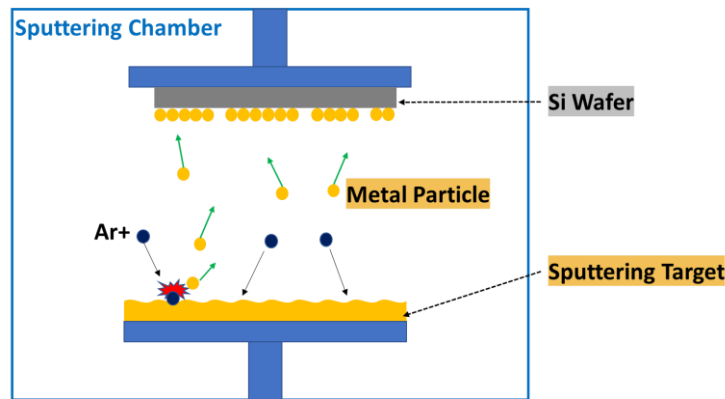


Fig. B. 4 - 1. The schematic of the metal sputtering deposition function of the Intlvac® Nanochrome Deposition System. [104]

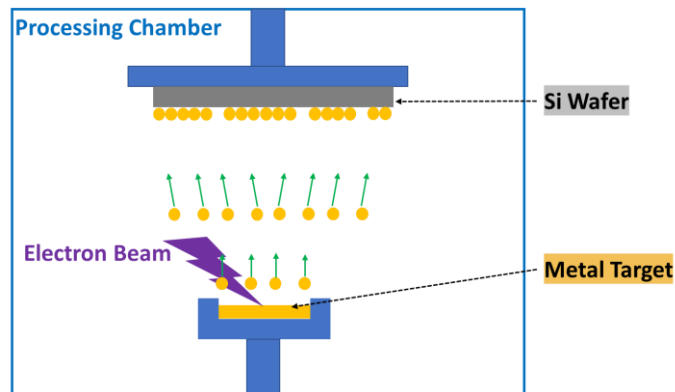


Fig. B. 4 - 2. The schematic of the e-beam evaporation deposition function of the Intlvac® Nanochrome Deposition System. [104]

Since the adhesion between silicon and gold is poor, gold cannot be directly deposited on a silicon wafer. To enhance the adhesion between the gold and Si, an adhesion metal layer is deposited on the etched Si wafer before coating the wafer with gold. Tungsten-titanium (TiW) is used as the adhesion metal layer. The metal plating coating process is shown in Fig. B.4-3. First, 80 nm thick TiW was sputtered on the Si wafer, after which an 80 nm thick gold layer was sputtered on the wafer by using the same deposition system. Finally, the thickness of the gold layer was increased to 3  $\mu\text{m}$  using the Technic® 5-Tank Electroplating System at CIRFE. Figure B.4-4 presents photos of an Si wafer coated with TiW and gold.

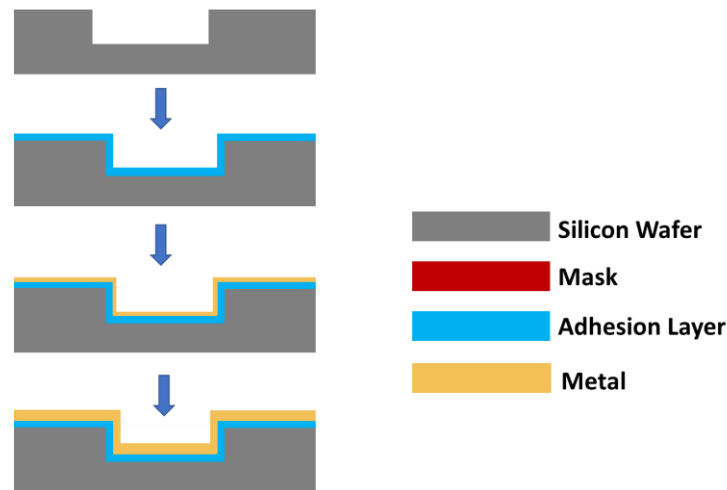


Fig. B. 4 - 3. The processes for coating gold layer on the Si wafer.

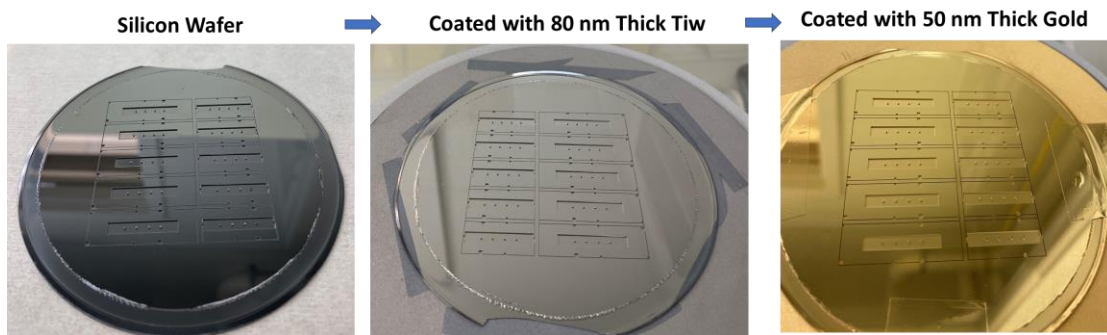


Fig. B. 4 - 4. A Si wafer is coated with 80 nm thick TiW as the adhesion metal layer and then 80 nm thick gold is sputtered on the wafer.